PROGRAMLANABİLİR DENETLEYİCİ
TEMEL KOMUTLAR İÇİN PROGRAMLAMA ÖRNEKLERİ

1. Input Circuit

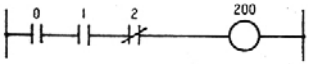
Instruction Word	No./Data
LOD	0
OUT	200

A LOD instruction is used to designate an input branched from the bus.

2. AND Circuit 1 (Series Circuit)

Instruction Word	No./Data
LOD·NOT	0
AND	1
OUT	200

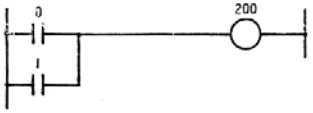
3. AND Circuit 2 (Series Circuit)



Instruction Word	No./Data
LOD	0
AND	1
AND·NOT	2
OUT	200

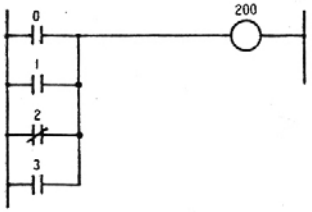
AND instructions can be used continuously without limitation.

4. OR Circuit 1 (Parallel Circuit)



Instruction Word	No./Data
LOD	0
OR	1
OUT	200

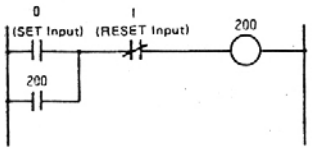
5. OR Circuit 2 (Parallel Circuit)



Instruction Word	No./Data
LOD	0
OR	1
OR·NOT	2
OR	3
OUT	200

OR instructions can be used continuously without limitation.

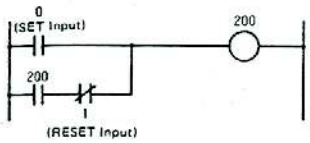
6. Self-Holding Circuit 1 (RESET Preferred)



Instruction Word	No./Data
LOD	0
OR	200
AND·NOT	1
OUT	200

Turning on SET input 0 while RESET input 1 is off turns on Output 200, which remains on after SET input 0 goes off.

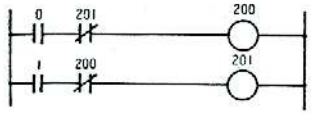
7. Self-Holding Circuit 2 (SET Preferred)



Instruction Word	No./Data
LOD	0
LOD	200
AND·NOT	1
OR·LOD	
OUT	200

Turning on SET input 0 turns on Output 200 whether RESET input is on or off, and Output 200 remains on after SET input 0 goes off.

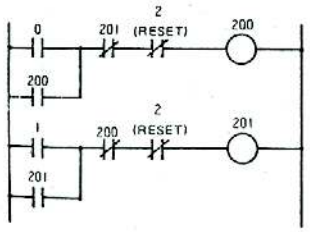
8. Priority Circuit 1 (Continuous Input Signal)



Instruction Word	No./Data
LOD	0
AND·NOT	201
OUT	200
LOD	1
AND·NOT	200
OUT	201

Input 0 or 1 whichever enters first is given priority, nullifying the input which enters next.

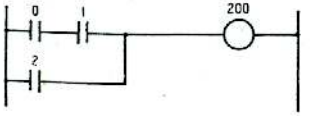
9. Priority Circuit 2 (Pulse Input Signal)



Instruction Word	No./Data
LOD	0
OR	200
AND·NOT	201
AND·NOT	2
OUT	200
LOD	1
OR	201
AND·NOT	200
AND·NOT	2
OUT	201

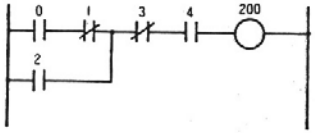
This circuit is used when outputs should be prevented from turning on simultaneously, such as forward/reverse control of a motor.

10. Series-Parallel Circuit 1



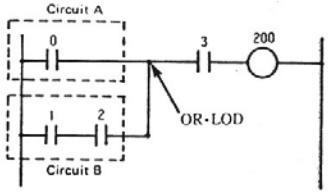
Instruction Word	No./Data
LOD	0
AND	1
OR	2
OUT	200

11. Series-Parallel Circuit 2



Instruction Word	No./Data
LOD	0
AND•NOT	1
OR	2
AND•NOT	3
AND	4
OUT	200

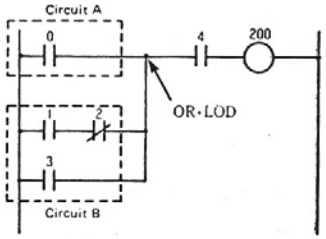
12. Series-Parallel (OR•LOD) Circuit 3



Instruction Word	No./Data	
LOD	0	- A
LOD	1	- B
AND	2	
OR•LOD		
AND	3	
OUT	200	

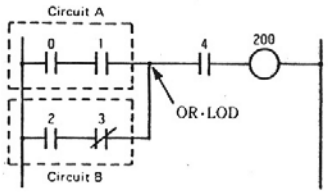
After Circuits A and B are programmed, these circuits are ORed by an OR•LOD instruction. Thereafter, AND3 instruction is programmed.

13. Series-Parallel (OR•LOD) Circuit 4



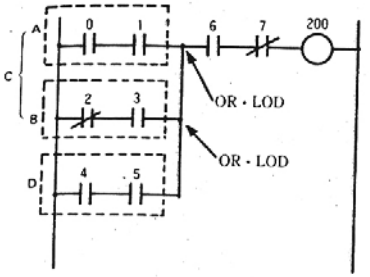
Instruction Word	No./Data	
LOD	0	- A
LOD	1	- B
AND•NOT	2	
OR	3	
OR•LOD		- OR circuit of A and B
AND	4	
OUT	200	

14. Series-Parallel (OR•LOD) Circuit 5



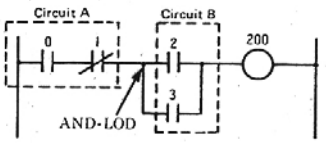
Instruction Word	No./Data	
LOD	0	- A
AND	1	
LOD	2	- B
AND•NOT	3	
OR•LOD		- OR circuit of A and B
AND	4	
OUT	200	

15. Series-Parallel (OR•LOD) Circuit 6



Instruction Word	No./Data		
LOD	0	- A	- C
AND	1		
LOD•NOT	2	- B	
AND	3		
OR•LOD		- OR circuit of A and B	
LOD	4	- D	
AND	5		
OR•LOD		- OR circuit of C and D	
AND	6		
AND•NOT	7		
OUT	200		

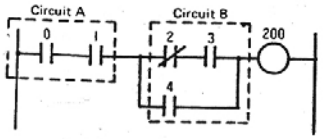
16. Series-Parallel (AND•LOD) Circuit 1



Instruction Word	No./Data	
LOD	0	- A
AND•NOT	1	
LOD	2	- B
OR	3	
AND•LOD		
OUT	200	

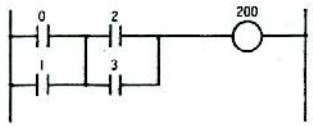
After Circuits A and B are programmed, these circuits are ANDed by an AND•LOD instruction.

17. Series-Parallel (AND•LOD) Circuit 2

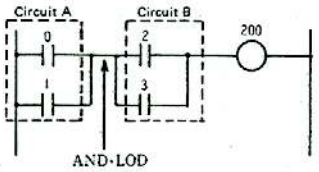


Instruction Word	No./Data		
LOD	0	- A	
AND	1		
LOD•NOT	2	- B	
AND	3		
OR	4		
AND•LOD		- AND circuit of A and B	
OUT	200		

18. Series-Parallel (AND·LOD) Circuit 3

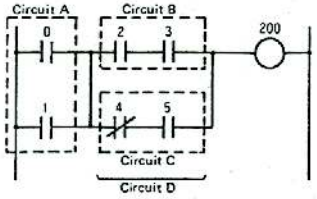


When modified, the circuit is easy to understand.



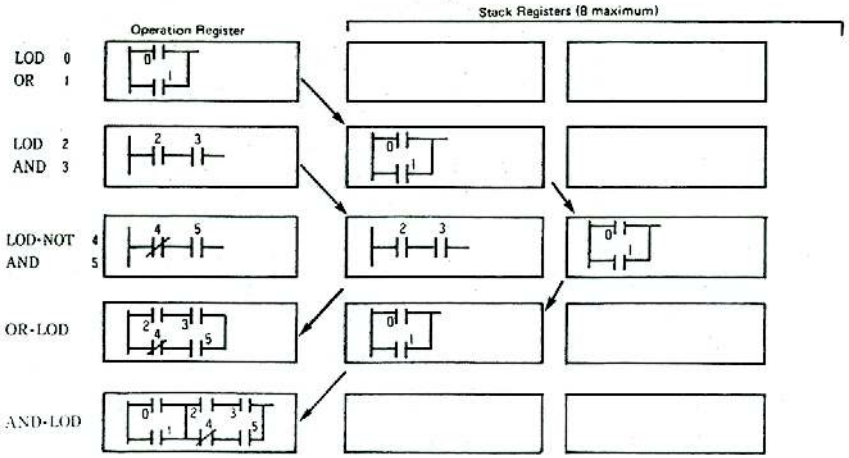
Instruction Word	No./Data	
LOD	0	- A
OR	1	
LOD	2	- B
OR	3	
AND·LOD		- AND circuit of A and B
OUT	200	

19. Series-Parallel (AND·LOD & OR·LOD) Circuit 4

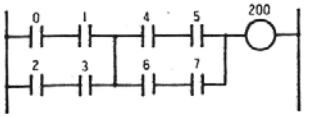


Instruction Word	No./Data	
LOD	0	A
OR	1	
LOD	2	B
AND	3	
LOD·NOT	4	C
AND	5	
OR·LOD		OR circuit of B and C = D
AND·LOD		AND circuit of A and D
OUT	200	

NOTE: Operations of Operation Registers and Stack Registers

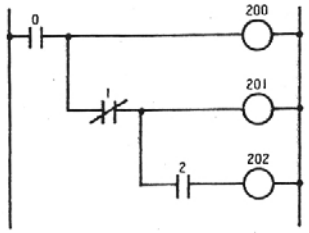


20. Series-Parallel (AND·LOD & OR·LOD) Circuit 5



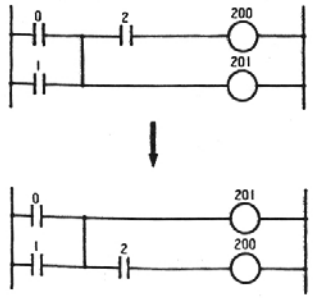
Instruction Word	No./Data
LOD	0
AND	1
LOD	2
AND	3
OR·LOD	
LOD	4
AND	5
LOD	6
AND	7
OR·LOD	
AND·LOD	
OUT	200

21. Multiple Output Circuit 1



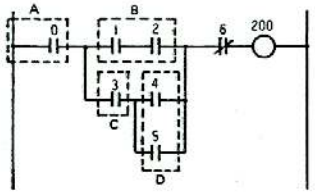
Instruction Word	No./Data
LOD	0
OUT	200
AND·NOT	1
OUT	201
AND	2
OUT	202

22. Multiple Output Circuit 2



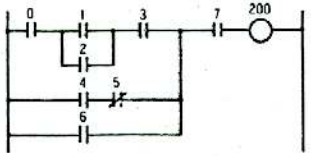
Instruction Word	No./Data
LOD	0
OR	1
OUT	201
AND	2
OUT	200

23. Complex Circuit 1



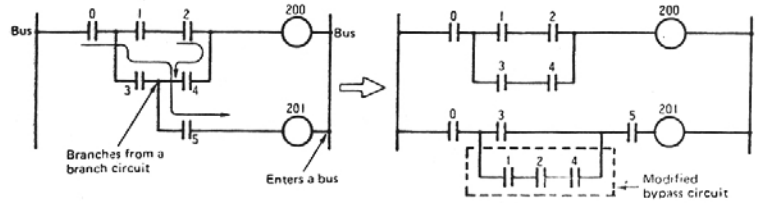
Instruction Word	No./Data	
LOD	0	- A
LOD	1	- B
AND	2	
LOD	3	- C
LOD	4	- D
OR	5	
AND•LOD		- AND circuit of C and D = E
OR•LOD		- OR circuit of B and E = F
AND•LOD		- AND circuit of A and F
AND•NOT	6	- AND-NOT 6 is added at the end.
OUT	200	

24. Complex Circuit 2



Instruction Word	No./Data
LOD	0
LOD	1
OR	2
AND•LOD	
AND	3
LOD	4
AND•NOT	5
OR•LOD	
OR	6
AND	7
OUT	200

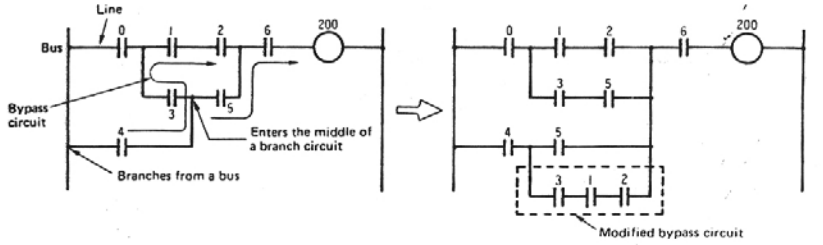
1. Branching from a Branch Circuit to a Bus



●Circuit which cannot be programmed

●Circuit modified for PC

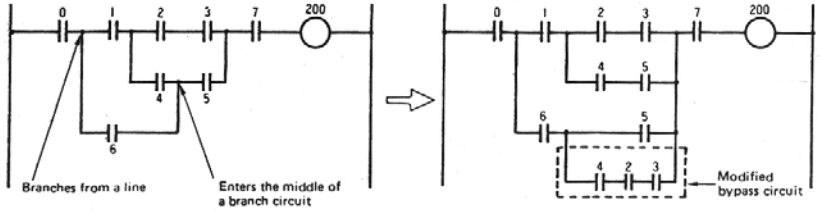
2. Branching from a Bus to the Middle of a Branch Circuit



●Circuit which cannot be programmed

●Circuit modified for PC

3. Branching from a Line to the Middle of a Branch Circuit

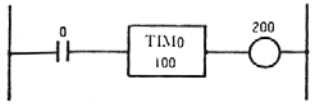


●Circuit which cannot be programmed

●Circuit modified for PC

1. ON-Delay Timer

(a)



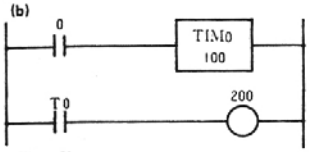
Instruction Word	No./Data
LOD	0
TIM	0
	100
OUT	200

A TIM instruction requires two addresses.

TIM No.

Preset time (100 = 10.0 sec)

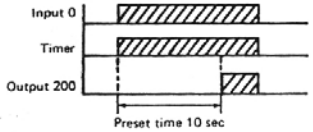
(b)



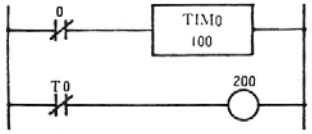
Instruction Word	No./Data
LOD	0
TIM	0
	100
LOD·T	0
OUT	200

TIM instructions can be programmed in two ways; 1. as with Circuit (a), output can be taken out directly from the TIM instruction, and 2. as with Circuit (b), output can be converted to a contact signal and taken out.

●Time Chart

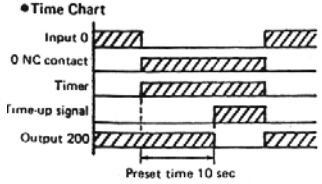


2. OFF-Delay Timer



Instruction Word	No./Data
LOD·NOT	0
TIM	0
	100
LOD·NOT·T	0
OUT	200

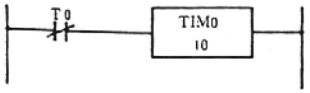
●Time Chart



When Input 0 goes off, the NC contact of Input 0 starts TIM 0. After a preset time, the NC contact of TIM 0 turns off Output 200.
When Input 0 goes on, Output 200 also goes on.

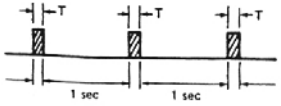
3. Pulse Generating Circuit

(a) Flicker Circuit



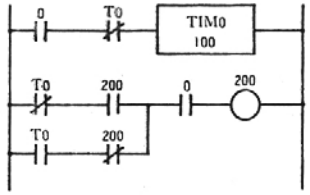
Instruction Word	No./Data
LOD·NOT·T	0
TIM	0
	10

●Time Chart



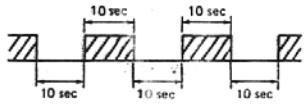
T = 1 scan time

(b) Constant Duty Ratio Pulse Generating Circuit



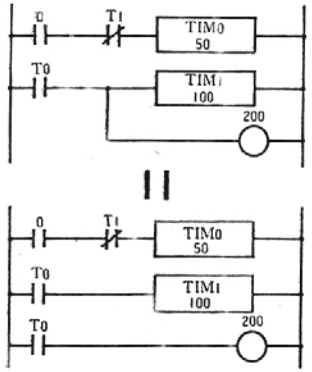
Instruction Word	No./Data
LOD	0
AND·NOT·T	0
TIM	0
	100
LOD·NOT·T	0
AND	200
LOD·T	0
AND·NOT	200
OR·LOD	
AND	0
OUT	200

●Time Chart



While Input 0 is on, output pulses with same ON and OFF durations (duty ratio 1:1) are generated.

(c) Adjustable Duty Ratio Pulse Generating Circuit

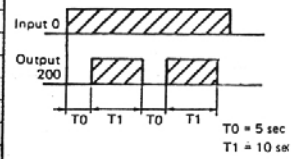


Instruction Word	No./Data
LOD	0
AND·NOT·T	1
TIM	0
	50
LOD·T	0
OUT	200
TIM	1
	100

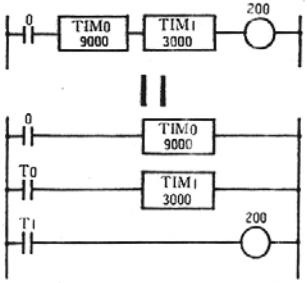
Instruction Word	No./Data
LOD	0
AND·NOT·T	1
TIM	0
	50
LOD·T	0
TIM	1
	100
LOD·T	0
OUT	200

While Input 0 is on, output pulses with OFF duration of TIM 0 and ON duration of TIM 1 are generated.
Output can be programmed in parallel with TIM instructions.

●Time Chart



4. Long-Delay Timer 1 (Timer + Timer)

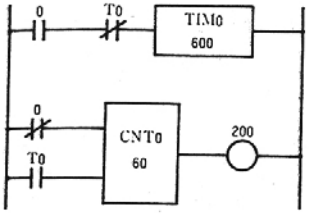


Instruction Word	No./Data	
LOD	0	
TIM	0	
	9000	900 sec
TIM	1	
	3000	300 sec
OUT	200	

TIM instructions can be programmed continuously to provide a long-delay timer.
There is no limit to the number of TIM instructions to be programmed continuously.

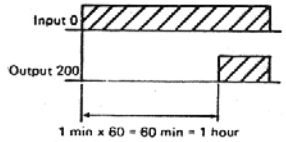
Example: 9000 (900 sec) + 3000 (300 sec) = 12000 (1200 sec) = 20

5. Long-Delay Timer 2 (Timer + Counter)



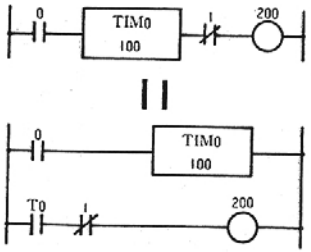
Instruction Word	No./Data	
LOD	0	
AND·NOT·T	0	
TIM	0	
	600	60 sec (1 min)
LOD·NOT	0	
LOD·T	0	
CNT	0	
	60	× 60
OUT	200	

●Time Chart



After Input 0 has turned on, clock pulses generated by TIM 0 are counted to provide a long-delay timer.

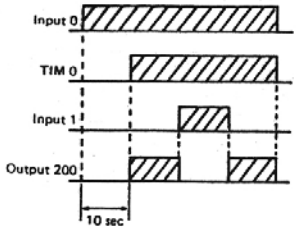
6. Circuit to Turn Output Off Temporarily after Time-up



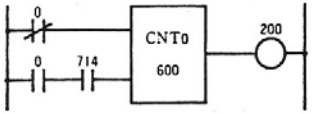
Instruction Word	No./Data
LOD	0
TIM	0
	100
AND·NOT	1
OUT	200

Following to a TIM instruction, a circuit can be programmed.

●Time Chart

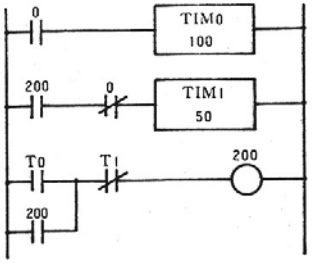


7. Timer Using Special Internal Relay IR 714 (1-sec clock)



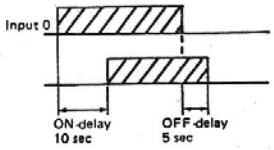
Instruction Word	No./Data	
LOD·NOT	0	
LOD	0	
AND	714	1-sec clock pulse
CNT	0	
	600	600 sec (10 min)
OUT	200	

8. ON/OFF Delay Circuit



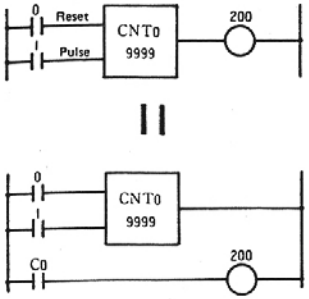
Instruction Word	No./Data	
LOD	0	
TIM	0	
	100	10 sec
LOD	200	
AND·NOT	0	
TIM	1	
	50	5 sec
LOD·T	0	
OR	200	
AND·NOT·T	1	
OUT	200	

●Time Chart



Output 200 turns on 10 sec after Input 0 has turned on, and Output 200 turns off 5 sec after Input 0 has turned off.

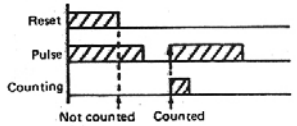
1. Adding Counter 1



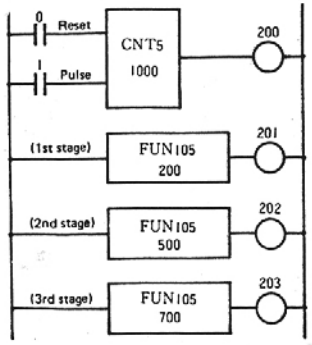
Instruction Word	No./Data
LOD	0
LOD	1
CNT	0
	9999 - Preset value
OUT	200

While Input 0 is off, Input 1 pulse signals are counted. When reaching the preset value, Output 200 is turned on.

●Pulse Input Acceptance Timing

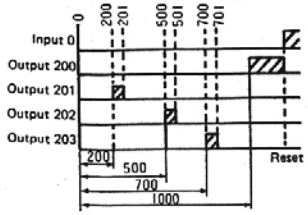


2. Adding Counter 2 (Multi-Stage Setting One-Shot Output Circuit)

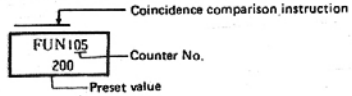


Instruction Word	No./Data
LOD	0
LOD	1
CNT	5
	1000 - Counter preset value
OUT	200
FUN	105 - 1st-stage setting
	200
OUT	201
FUN	105 - 2nd-stage setting
	500
OUT	202
FUN	105 - 3rd-stage setting
	700
OUT	203

●Time Chart

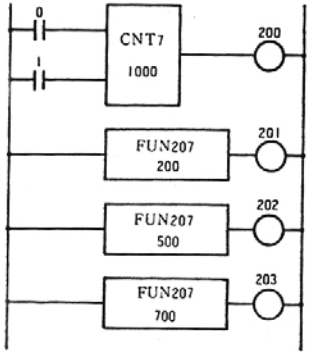


The multi-stage one-shot output circuit for the adding counter is programmed using a FUN□□ instruction (counter coincidence comparison instruction).
There is no limit to the number of stages for a multi-stage counter.



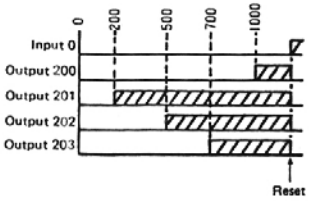
Output signal is on only when the counted value coincides with the preset value.

3. Adding Counter 3 (Multi-Stage Setting Self-Holding Output Circuit)

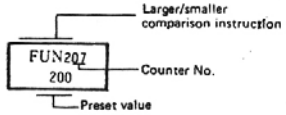


Instruction Word	No./Data
LOD	0
LOD	1
CNT	7
	1000 - Counter preset value
OUT	200
FUN	207 - 1st-stage setting
	200
OUT	201
FUN	207 - 2nd-stage setting
	500
OUT	202
FUN	207 - 3rd-stage setting
	700
OUT	203

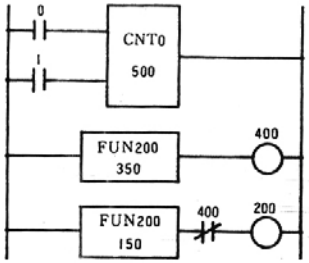
●Time Chart



The multi-stage self-holding output circuit for the adding counter is programmed using a FUN2□□ instruction (counter larger/smaller comparison instruction).
There is no limit to the number of stages for the multi-stage counter.



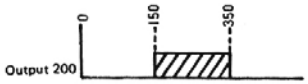
4. Adding Counter 4 (Larger/Smaller Comparison Circuit)



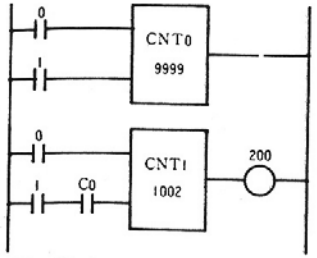
Instruction Word	No./Data
LOD	0
LOD	1
CNT	0
	500
FUN	200
	350
OUT	400
FUN	200
	150
AND·NOT	400
OUT	200

Output 200 is turned on when the counted value of Counter 0 is between 150 and 300.

●Time Chart



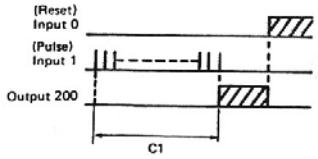
5. Multi-Digit Counter 1



Instruction Word	No./Data
LOD	0
LOD	1
CNT	0
	9999
LOD	0
LOD	1
AND·CNT	0
CNT	1
	1002
OUT	200

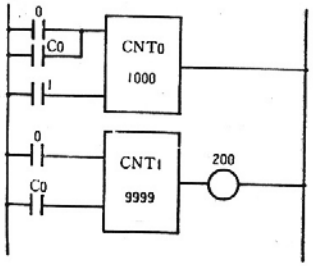
When the preset value exceeds 9999, two counters can be used to count up to 19997.

●Time Chart



$C1 = \underset{\text{value}}{\text{CNT 0 preset}} + \underset{\text{value}}{\text{CNT 1 preset}} - 1 = 9{,}999 + 1{,}002 - 1 = 11{,}000$

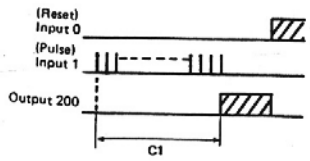
6. Multi-Digit Counter 2 (7-Digit Setting)



Instruction Word	No./Data
LOD	0
OR·C	0
LOD	1
CNT	0
	1000
LOD	0
LOD·C	0
CNT	1
	9999
OUT	200

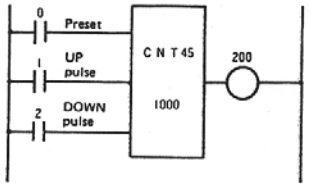
When the preset value exceeds 4 digits, two counters can be used to provide a 7-digit counter.

●Time Chart



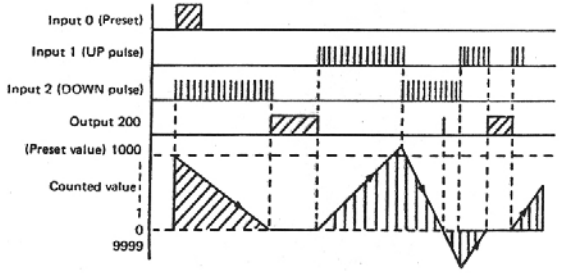
$C1 = \underset{\text{value}}{\text{CNT 0 preset}} \times \underset{\text{value}}{\text{CNT 1 preset}} = 1{,}000 \times 9{,}999 = 9{,}999{,}000$

6. Dual-Pulse Type Reversible Counter Circuit (CNT 45)



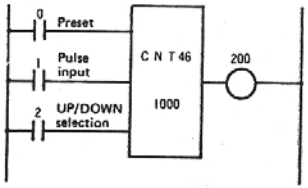
Instruction Word	No./Data
LOD	0
LOD	1
LOD	2
CNT	45
	1000
OUT	200

This reversible counter has two pulse inputs for adding (UP) and subtracting (DOWN).



UP and DOWN pulse inputs are accepted. When Preset input 0 enters, the counted value is reset to the CNT 45 preset value (1000). Output 200 is on only when the counted value is 0.

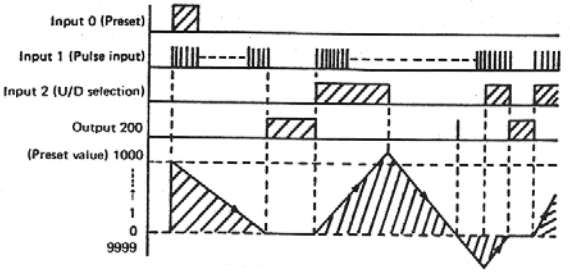
7. UP/DOWN Selection Type Reversible Counter Circuit (CNT 46 & 47)



Instruction Word	No./Data
LOD	0
LOD	1
LOD	2
CNT	46
	1000
OUT	200

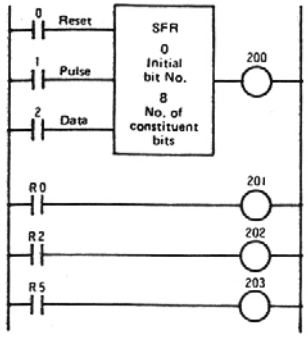
This reversible counter has a pulse input and a selection input for switching the UP/DOWN gate.

UP/DOWN selection input
ON: UP (adding)
OFF: DOWN (subtracting)

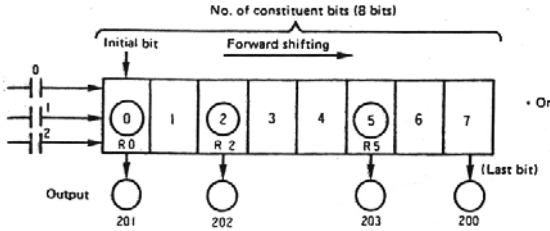


When Preset input 0 enters, the counted value is reset to the CNT 46 preset value (1000). Output 200 is on only when the counted value is 0.

1. Forward Shift Register Circuit

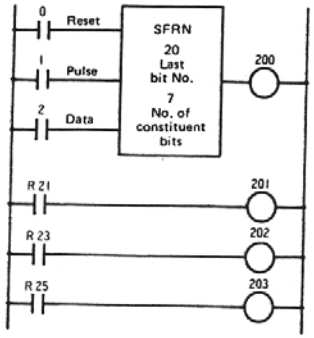


Instruction Word	No./Data	
LOD	0	
LOD	1	
LOD	2	
SFR	0	- Initial bit
	8	- 8-bit configuration
OUT	200	
LOD·R	0	- Deriving Bit 0 status
OUT	201	
LOD·R	2	- Deriving Bit 2 status
OUT	202	
LOD·R	5	- Deriving Bit 5 status
OUT	203	

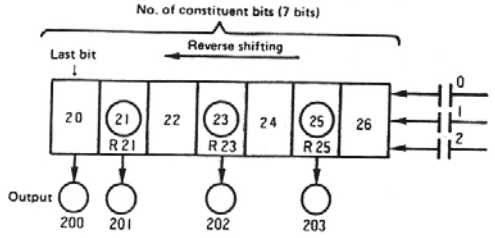


• Only the circled bits are outputted.

2. Reverse Shift Register Circuit

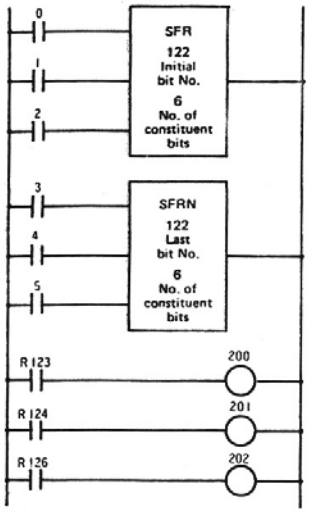


Instruction Word	No./Data	
LOD	0	
LOD	1	
LOD	2	
SFR·NOT	20	- Last bit
	7	- 7-bit configuration
OUT	200	
LOD·R	21	- Deriving Bit 21 status
OUT	201	
LOD·R	23	- Deriving Bit 23 status
OUT	202	
LOD·R	25	- Deriving Bit 25 status
OUT	203	

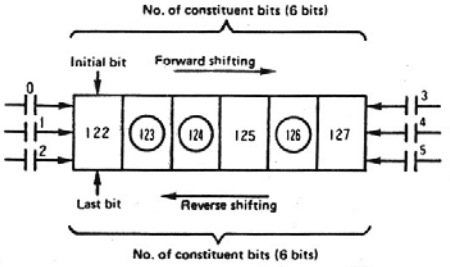


• Only the circled bits are outputted.

3. Bidirectional Shift Register Circuit



Instruction Word	No./Data
LOD	0
LOD	1
LOD	2
SFR	122
	6
LOD	3
LOD	4
LOD	5
SFR·NOT	122
	6
LOD·R	123
OUT	200
LOD·R	124
OUT	201
LOD·R	126
OUT	202



• Only the circled bits are outputted.