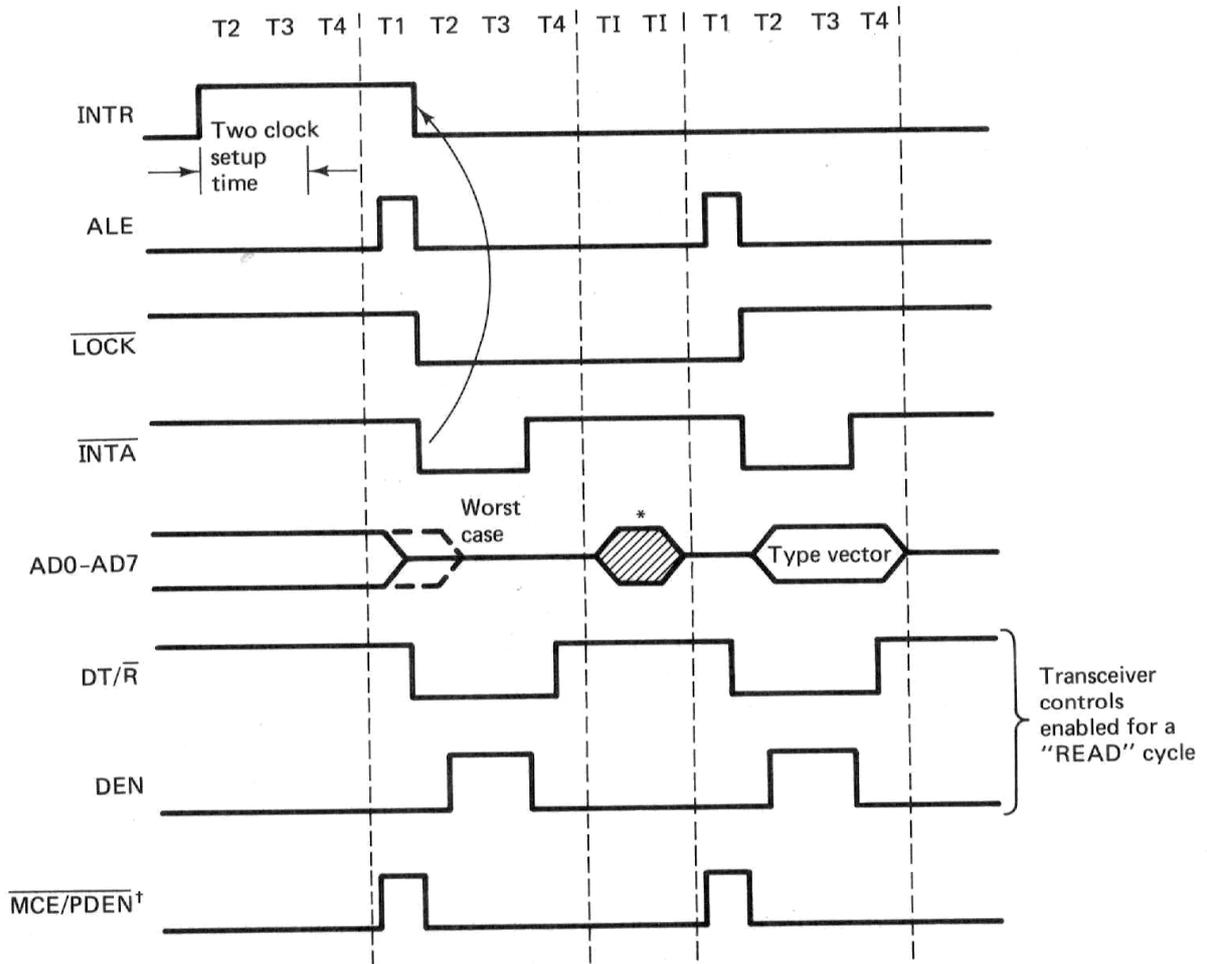**TABLE 8.5** 8086 INTERRUPT TYPES[a]

Name	Initiated by:	Maskable?	Trigger	Priority	Acknowledge signal?	Vector table address	Interrupt latency
NMI	External hardware	No	↑ Edge, hold 2 T states min.	2	None	00008H–0000BH	Current instruction + 51 T states
INTR	External hardware	Yes via IF	High level until acknowledged	3	$\overline{INTA}$	n * 4[b]	Current instruction + 61 T states
INT n	Internal via software	No	None	1	None	n * 4	51 T states
INT 3 (breakpoint)	Internal via software	No	None	1	None	0000CH–0000FH	52 T states
INTO	Internal via software	No	None	1	None	00010H–00013H	53 T states
Divide-by-0	Internal via CPU	Yes via OF	None	1	None	00000H–00003H	51 T states
Single-step	Internal via CPU	Yes via TF	None	4	None	00004H–00007H	51 T states

[a] All interrupt types cause the flags, CS, and IP registers to be pushed onto the stack. In addition, the IF and TF flags are cleared.

[b] n is an 8-bit type number read during the second INTA pulse.

+5 V

1 kΩ

8086

D   S   Q

INTR

Interrupt request

(ACKNLG)

RESET

INTA

(a)

AD7

AD6

AD5

+5 V 1 kΩ

AD4

AD3

n = 01000001 = 41H

AD2

AD1

AD0

LOCK

INTA

T2 T3 T4 | T1 T2 T3 T4 | TI TI | T1 T2 T3 T4 |

INTR — Two clock setup time

ALE

$\overline{\text{LOCK}}$

$\overline{\text{INTA}}$

AD0–AD7 — Worst case — * — Type vector

DT/$\overline{\text{R}}$

DEN

} Transceiver controls enabled for a "READ" cycle

$\overline{\text{MCE/PDEN}}$†

* Redriven by CPU if queue is not full
† Used to enable master 8259A PIC cascade address onto local bus