

## Microprocessor With Clock and Optional RAM

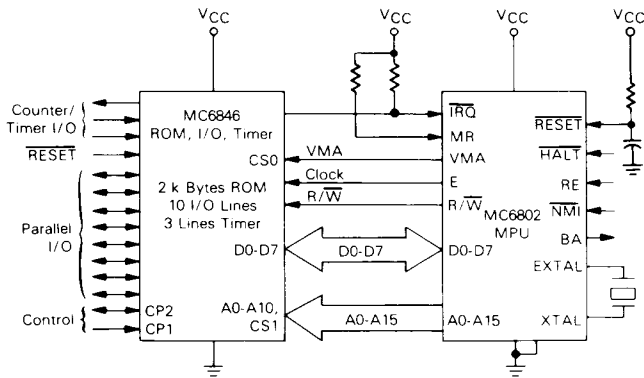
The MC6802 is a monolithic 8-bit microprocessor that contains all the registers and accumulators of the present MC6800 plus an internal clock oscillator and driver on the same chip. In addition, the MC6802 has 128 bytes of on-board RAM located at hex addresses \$0000 to \$007F. The first 32 bytes of RAM, at hex addresses \$0000 to \$001F, may be retained in a low power mode by utilizing VCC standby; thus, facilitating memory retention during a power-down situation.

The MC6802 is completely software compatible with the MC6800 as well as the entire M6800 family of parts. Hence, the MC6802 is expandable to 64K words.

- On-Chip Clock Circuit
- 128 × 8 Bit On-Chip RAM
- 32 Bytes of RAM are Retainable
- Software-Compatible with the MC6800
- Expandable to 64K Words
- Standard TTL-Compatible Inputs and Outputs
- 8-Bit Word Size
- 16-Bit Memory Addressing
- Interrupt Capability

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**TYPICAL MICROCOMPUTER**



This block diagram shows a typical cost effective microcomputer. The MPU is the center of the microcomputer system and is shown in a minimum system interfacing with a ROM combination chip. It is not intended that this system be limited to this function but that it be expandable with other parts in the M6800 Microcomputer family.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V <sub>CC</sub>	-0.3 to +7.0	V
Input Voltage	V <sub>in</sub>	-0.3 to +7.0	V
Operating Temperature Range MC6802, MC680A02, MC680B02 MC6802C, MC680A02C	T <sub>A</sub>	0 to +70 -40 to +85	°C
Storage Temperature Range	T <sub>stg</sub>	-55 to +150	°C

This input contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V<sub>SS</sub> or V<sub>CC</sub>).

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Average Thermal Resistance (Junction to Ambient) Plastic	θ <sub>JA</sub>	100	°C/W

## POWER CONSIDERATIONS

The average chip-junction temperature, T<sub>J</sub>, in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA}) \quad (1)$$

where:

- T<sub>A</sub> = Ambient Temperature, °C
- θ<sub>JA</sub> = Package Thermal Resistance, Junction-to-Ambient, °C/W
- P<sub>D</sub> = P<sub>INT</sub> + P<sub>PORT</sub>
- P<sub>INT</sub> = I<sub>CC</sub> × V<sub>CC</sub>, Watts — Chip Internal Power
- P<sub>PORT</sub> = Port Power Dissipation, Watts — User Determined

For most applications P<sub>PORT</sub> < P<sub>INT</sub> and can be neglected. P<sub>PORT</sub> may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P<sub>D</sub> and T<sub>J</sub> (if P<sub>PORT</sub> is neglected) is:

$$P_D = K \cdot (T_J + 273^\circ\text{C}) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \cdot (T_A + 273^\circ\text{C}) + \theta_{JA} \cdot P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P<sub>D</sub> (at equilibrium) for a known T<sub>A</sub>. Using this value of K, the values of P<sub>D</sub> and T<sub>J</sub> can be obtained by solving equations (1) and (2) iteratively for any value of T<sub>A</sub>.

**DC ELECTRICAL CHARACTERISTICS** ( $V_{DD} = +5.0 \text{ Vdc} \pm 0.5\%$ ,  $V_{SS} = 0$ ,  $T_A = 0$  to  $70^\circ\text{C}$ , unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Input High Voltage	Logic, EXTAL, RESET	$V_{IH}$	$V_{SS} + 2.0$ $V_{SS} + 4.0$	—	$V_{CC}$ $V_{CC}$	V
Input Low Voltage	Logic, EXTAL, RESET	$V_{IL}$	$V_{SS} - 0.3$	—	$V_{SS} + 0.8$	V
Input Leakage Current ( $V_{in} = 0$ to $5.25 \text{ V}$ , $V_{DD} = \text{max}$ )	Logic	$I_{in}$	—	1.0	2.5	$\mu\text{A}$
Output High Voltage ( $I_{Load} = -205 \mu\text{A}$ , $V_{CC} = \text{min}$ ) ( $I_{Load} = -145 \mu\text{A}$ , $V_{CC} = \text{min}$ ) ( $I_{Load} = -100 \mu\text{A}$ , $V_{CC} = \text{min}$ )	D0-D7 A0-A15, R/W, VMA, E BA	$V_{OH}$	$V_{SS} + 2.4$ $V_{SS} + 2.4$ $V_{SS} + 2.4$	— — —	— — —	V
Output Low Voltage ( $I_{Load} = 1.6 \text{ mA}$ , $V_{CC} = \text{min}$ )		$V_{OL}$	—	—	$V_{SS} + 0.4$	V
Internal Power Dissipation (Measured at $T_A = 0^\circ\text{C}$ )		$P_{INT}$	—	0.750	1.0	W
$V_{DD}$ Standby	Power Down Power Up	$V_{SBB}$ $V_{SB}$	4.0 4.75	— —	5.25 5.25	V
Standby Current		$I_{SBB}$	—	—	8.0	mA
Capacitance # ( $V_{in} = 0$ , $T_A = 25^\circ\text{C}$ , $f = 1.0 \text{ MHz}$ )	D0-D7 Logic Inputs, EXTAL A0-A15, R/W, VMA	$C_{in}$  $C_{out}$	— — —	10 6.5 —	12.5 10 12	pF

\*In power-down mode, maximum power dissipation is less than 42 mW.

#Capacitances are periodically sampled rather than 100% tested.

**CONTROL TIMING** ( $V_{CC} = 5.0 \text{ V} \pm 5\%$ ,  $V_{SS} = 0$ ,  $T_A = T_L$  to  $T_H$ ), unless otherwise noted)

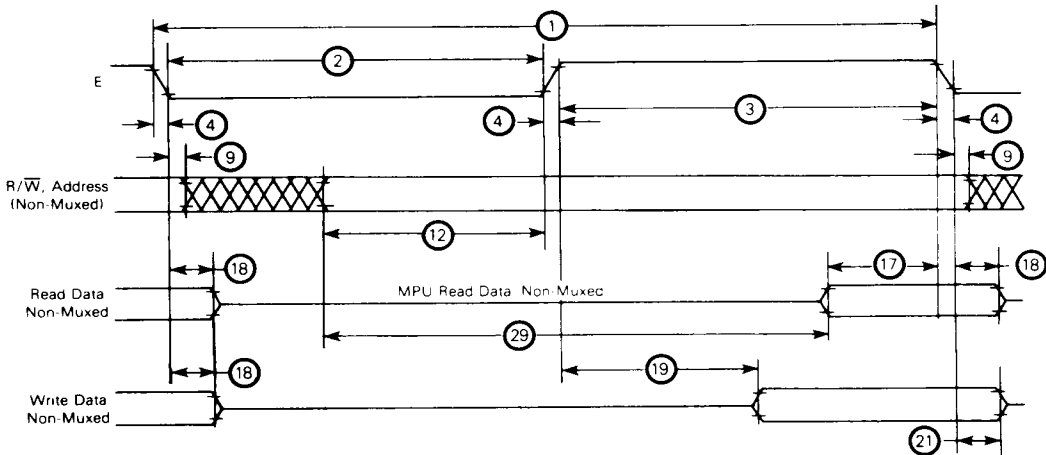
Characteristic	Symbol	MC6802		MC68A02		MC68B02		Unit
		Min	Max	Min	Max	Min	Max	
Frequency of Operation	$f_o$	0.1	1.0	0.1	1.5	0.1	2.0	MHz
Crystal Frequency	$f_{XTAL}$	1.0	4.0	1.0	6.0	1.0	8.0	MHz
External Oscillator Frequency	$4xf_o$	0.4	4.0	0.4	6.0	0.4	8.0	MHz
Crystal Oscillator Start Up Time	$t_{rc}$	100	—	100	—	100	—	ms
Processor Controls (HALT, MR, RE, RESET, IRQ NMI) Processor Control Setup Time Processor Control Rise and Fall Time (Does Not Apply to RESET)	$t_{PCS}$ $t_{PCr}$ $t_{PCf}$	200 — —	— 100 —	140 — —	— 100 —	110 — —	— 100 —	ns

BUS TIMING CHARACTERISTICS

Ident. Number	Characteristic	Symbol	MC6802		MC68A02		MC68B02		Unit
			Min	Max	Min	Max	Min	Max	
1	Cycle Time	$t_{cyc}$	1.0	10	0.667	10	0.5	10	$\mu s$
2	Pulse Width, E Low	PWEL	450	5000	280	5000	210	5000	ns
3	Pulse Width, E High	PWEH	450	9500	280	9700	220	9700	ns
4	Clock Rise and Fall Time	$t_r, t_f$	—	25	—	25	—	25	ns
9	Address Hold Time*	$t_{AH}$	20	—	20	—	20	—	ns
12	Non-Muxed Address Valid Time to E (see Note 4)	$t_{AV1}$ $t_{AV2}$	160	—	100	—	50	—	ns
17	Read Data Setup Time	$t_{DSR}$	100	—	70	—	60	—	ns
18	Read Data Hold Time	$t_{DHR}$	10	—	10	—	10	—	ns
19	Write Data Delay Time	$t_{DDW}$	—	225	—	170	—	160	ns
21	Write Data Hold Time*	$t_{DHW}$	30	—	20	—	20	—	ns
29	Usable Access Time (see Note 4)	$t_{ACC}$	535	—	335	—	235	—	ns

\*Address and data hold times are periodically tested rather than 100% tested.

FIGURE 2 — BUS TIMING



NOTES:

1. Voltage levels shown are  $V_L = 0.4 V$ ,  $V_H \geq 2.4 V$ , unless otherwise specified.
2. Measurement points shown are 0.8 V and 2.0 V, unless otherwise noted.
3. Usable access time is computed by:  $12 + 3 + 4 - 17$ .
4. If programs are not executed from on-board RAM,  $T_{AV1}$  applies. If programs are to be stored and executed from on-board RAM,  $T_{AV2}$  applies. For normal data storage in the on-board RAM, this extended delay does not apply. Programs cannot be executed from on-board RAM when using A and B parts (MC68A02, MC68B02). On-board RAM can be used for data storage with all parts.
5. All electrical and control characteristics are referenced from:  $T_L = 0^\circ C$  minimum and  $T_H = 70^\circ C$  maximum.

