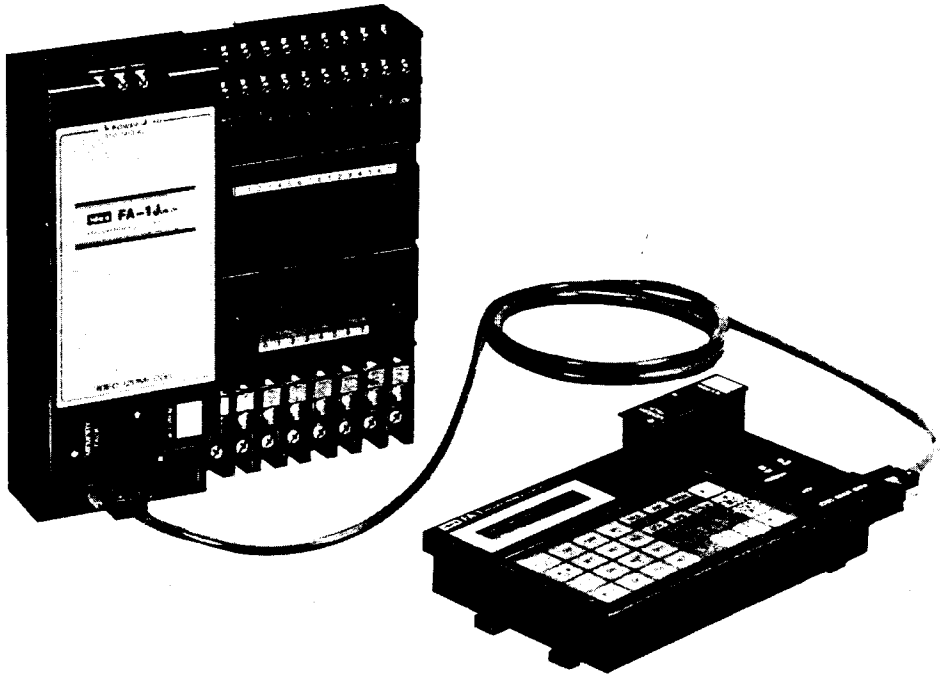
USERS MANUAL EM043-6

JUNIOR

FA-1 JUNIOR SERIES PROGRAMMABLE CONTROLLER

USERS MANUAL



idec IDEC IZUMI CORPORATION

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Chapter 1 — UNIT

FEATURES

Thin Flat Housing

The FA-1J is a high-performance multi-function programmable controller featuring a thin flat space-saving housing suited for small and shallow control boards requiring high-density component installation.

Effective Expansion up to 256 I/Os

Since CPU and I/O units have a modular configuration, the number of inputs and outputs can be expanded from 16 up to 256 by a unit of 8 or 16 points.

Memory Packs for Easy Memory Change

The FA-1J features a plug-in memory pack which can be easily replaced to change and store programs. Three types of memory packs are available to meet your specific needs.

Multi-Function Program Loader

The detachable program loader can be used in many ways; connected to the CPU unit with an extension cable for hand-held programming and can be mounted on a panel. The loader can be used separately at the office for remote programming with the use of an AC adapter.
In addition, the program loader features a PROM programming function and audio cassette interface.

AC and DC Power Voltage Types

The FA-1J is available in two power voltage types; 100 to 240V AC free power type and 24V DC type. If only AC or DC type I/O units are used, the entire control system can be operated from an AC or DC power.

Computing Function

Computing functions such as adding, subtracting, multiplying, dividing, BCD-to-binary conversion, binary-to-BCD conversion, and numerical comparison (4 digits) allow complex control to be performed by simple programming.

Multiple Functions

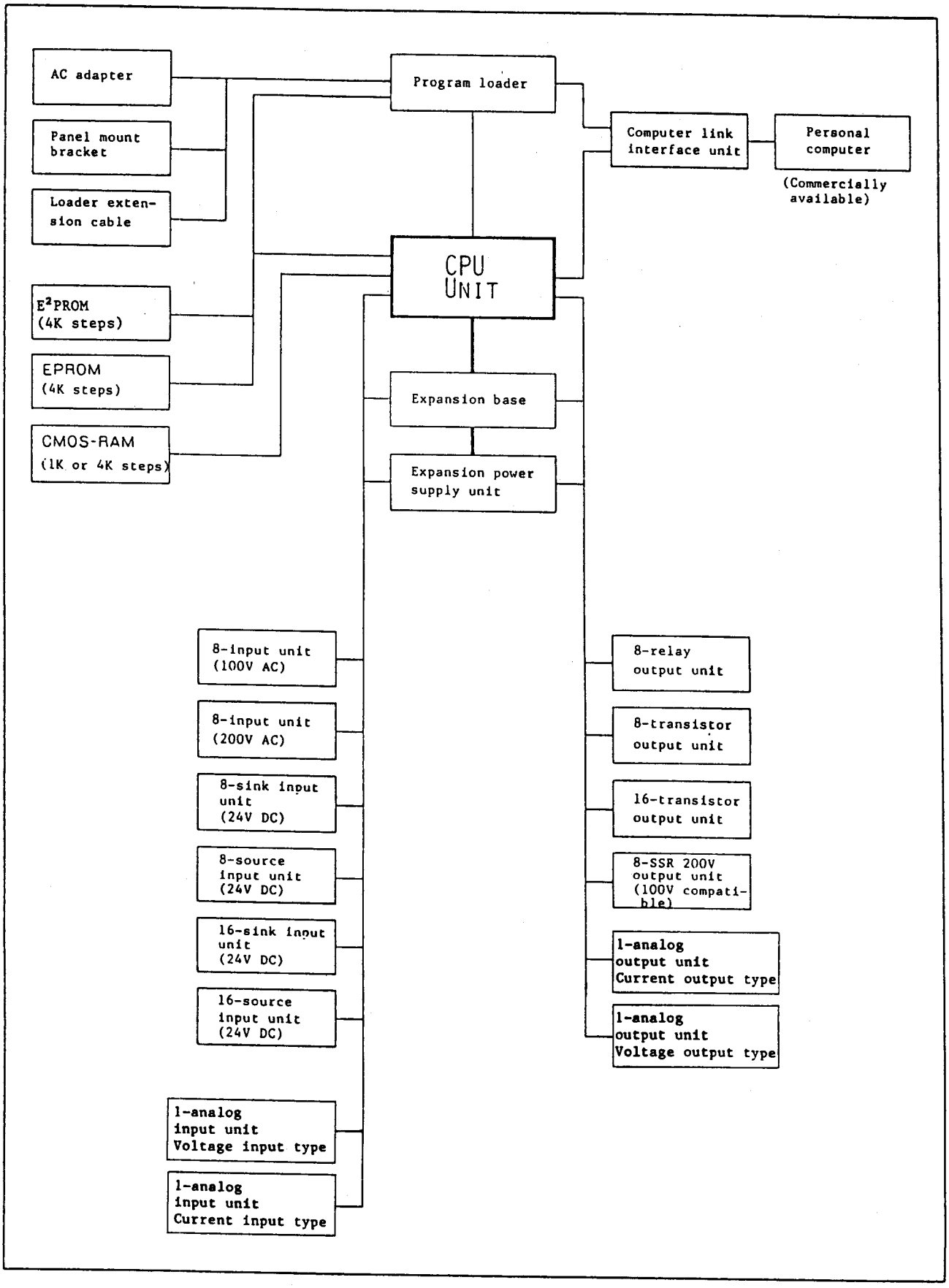
The FA-1J features multiple functions to meet various control requirements, such as reversible counter, bidirectional shift register, timer/counter preset value change during PROM operation, program shift using a JUMP function, and external digital display/preset using I/O units.

Computer Link

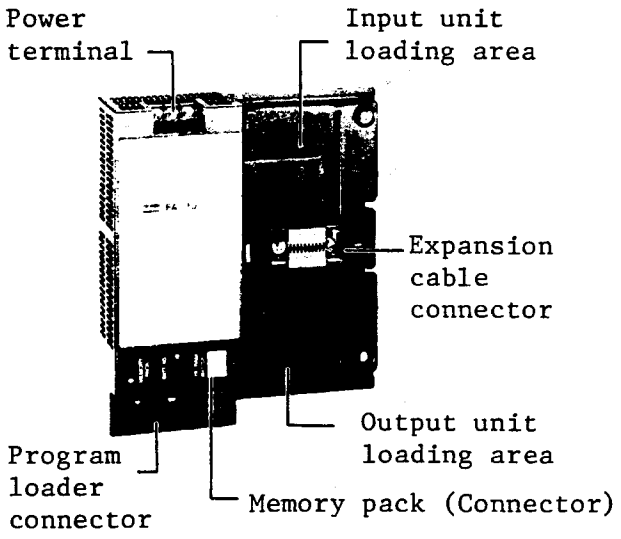
The FA-1J can be easily linked to a personal computer to make a total control system. A standard program for IBM 5150 and 5160 personal computers is optionally available for printing out programs using a personal computer.

SYSTEM CONFIGURATION

Configuration Block Diagram



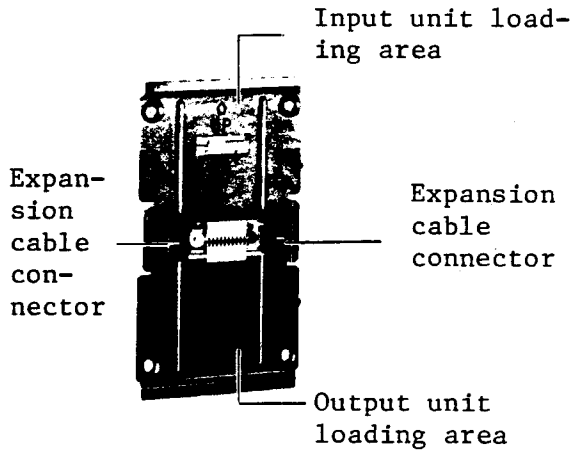
CPU Unit



- PFJ-CR1E : Power voltage 100V to 240V AC
- PFJ-CR1DCE: Power voltage 24V DC

This base unit with a built-in CPU is used in combination with input/output units. Two input or output units can be loaded on one CPU unit.
Memory packs are ordered separately.

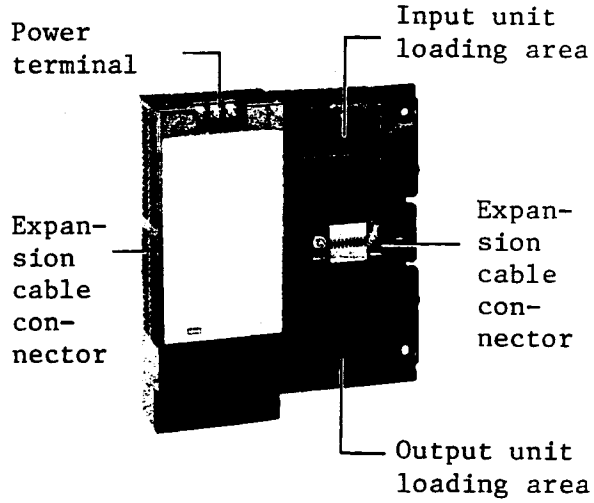
Expansion Base



- PFJ-EB1

This expansion base is used for expansion of input and output units. Two input or output units can be loaded on one expansion base.

Expansion Power Supply Unit

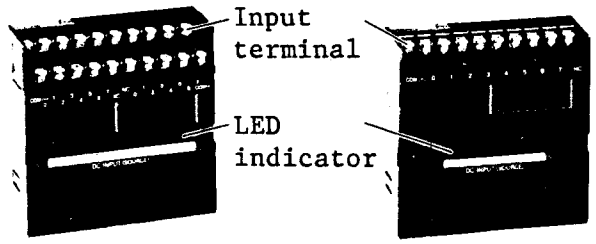


- PFJ-PS1 : Power voltage 100V to 240V AC
- PFJ-PS1DC: Power voltage 24V DC

This unit is connected for expansion of input or output units, if necessary. Two input or output units can be loaded on one expansion power supply unit.

DC Input Unit

(16-input type) (8-input type)



(Source type)

- PFJ-N161: 16 inputs
- PFJ-N081: 8 inputs

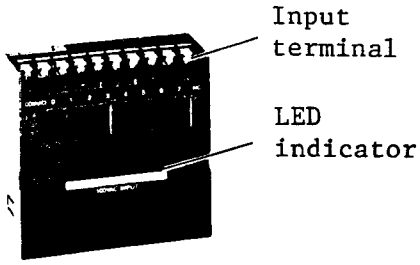
This unit is used in combination with the CPU unit. It is compatible with NPN-output sensors.

(Sink type)

- PFJ-N162: 16 inputs
- PFJ-N082: 8 inputs

This unit is used in combination with the CPU unit. It is compatible with PNP-output sensors.

AC Input Unit



- PFJ-N083: 8 inputs

This unit is used in combination with the CPU unit. It accepts voltage inputs of 100V AC.

- PFJ-N084: 8 inputs

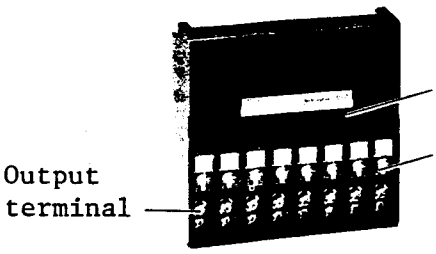
This unit is used in combination with the CPU unit. It accepts voltage inputs of 200V AC.

Analog Input Unit

- PFJ-N012: Voltage input type
- PFJ-N013: Current input type

The analog input unit converts an analog signal of 0-10V or 4-20mA DC into an 8-bit binary value to be accepted by the FA-1 input.

Relay Output Unit

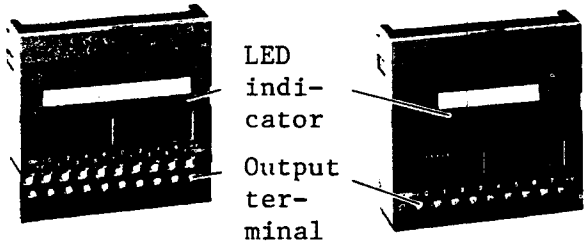


- PFJ-T081: 8 outputs

This unit is used in combination with the CPU unit. IDEC's miniature relays (5A-110V AC) are provided as standard. Each relay can be replaced with a transistor or SSR output module.

Transistor Output Unit

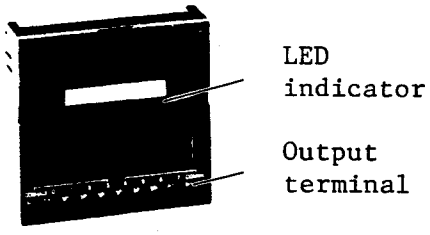
(16-output type) (8-output type)



- PFJ-T162: 16 outputs
- PFJ-T082: 8 outputs

This unit is used in combination with the CPU unit. The rated load is 24V DC 0.5A (PFJ-T162), or 48V DC 1.0A (PFJ-T082).

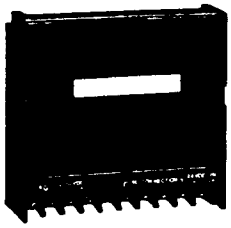
SSR Output Unit



- PFJ-T083: 8 outputs

This unit is used in combination with the CPU unit. The rated load is 200V AC 1.0A. (It can operate a load of 100V AC.)

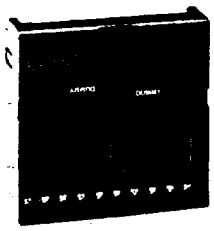
Analog Output Unit



- PFJ-T012: Voltage output type
- PFJ-T013: Current output type

The analog output unit converts 8-bit data processed in the FA-1J into analog output signals of 0-10V or 4-20mA DC.

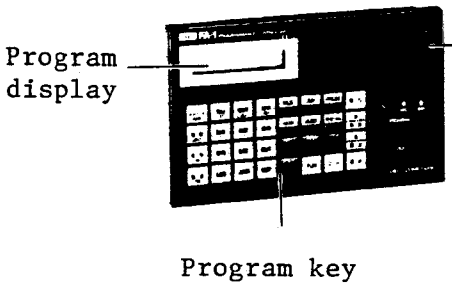
Dummy Unit



- PFJ-DM

This unit is loaded to fill the void in place of input or output units on the base.

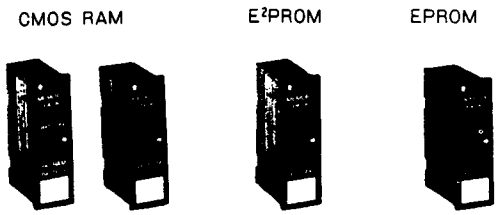
Program Loader



- PFA-1H401RE (1K steps)
- PFA-1H404RE (4K steps)

This multifunctional program loader with a built-in CPU is provided with both programming and PROM writing functions.

Memory Pack



The memory pack is used to write, read and store programs. One memory pack is always required for one control system. (Since the CPU unit is not equipped with a memory pack, a separate order is required.)

General Specifications

Power Voltage	100 to 240V AC, +10 to -15%, 50/60Hz 24V DC ±20% (Ripple 10% maximum)
Storage Temperature	-20 to +70°C
Operating Temperature	0 to +55°C
Operating Humidity	45 to 85% RH (no condensation)
Dielectric Strength	Between power or I/O terminal and housing: 1,500V AC 1 minute (5.0mA maximum)
Insulation Resistance (measured with a 500V DC megger)	Between power or output terminal and housing: 10MΩ minimum
Vibration Resistance	16.7Hz 2G, 1 hour each in 3 axes
Shock Resistance	10G
Noise Resistance	Power noise: ±1,300V (AC), ±1,000V (DC) I/O noise : ±1,300V (with a 1-μsec pulse generator)
Operating Atmosphere	Free from corrosive gases
Mounting Style	Wall
Power Consumption and Weight (Approx.)	CPU unit 45VA (AC), 25W (DC): 1 kg Program loader 3.2W : 0.4 kg

Function Specifications

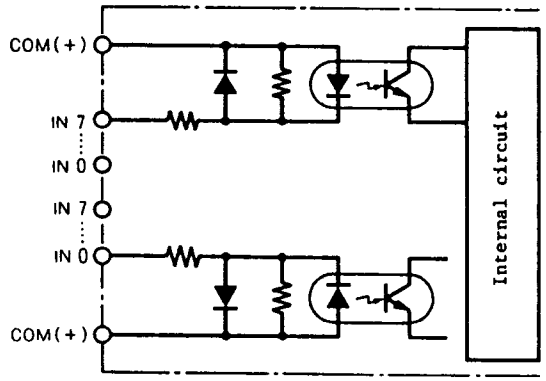
Control System	Stored program system
Programming Method	Logic symbol
Instruction Word	15 basic instructions, 27 applied instructions
Program Capacity	1K steps (964 steps), 4K steps (4036 steps)
Memory Pack	CMOS-RAM (with battery) 1K, 4K steps E^2PROM 4K steps EPROM 4K steps
Scan Time	32msec/1K steps
Input	128 points max., 8 points min. (One point is start terminal.)
Output	128 points max., 8 points min.
Internal Relay	240 points (All points can be maintained.)
Special Internal Relay	16 points
Shift Register	128 points (All points can be maintained.)
Single Output	96 points
Timer	80 points, subtracting (0 to 999.9 sec)
Counter	45 points, adding (0 to 9999) (All points can be maintained.)
Reversible Counter	2 points (All points can be maintained.)
Computer Link	Via the RS232C interface unit
External Control Input	Start : Input No. 0 (fixed) Stop & Reset: Designated by FUN
Power Failure Protection	Internal relay, Shift register, Counter, Reversible counter
Self-Diagnostic Function	CPU error (WDT), transmission error, CRC on user programs, operation code error
Power Supply for I/O Unit*	650mA (CPU unit) 1,100mA (Expansion power supply unit)
Automatic Start Function	Designated by FUN to start operation when turning power on

Note*: This power supply cannot be used as an external power supply for input sensors.

Input Specifications

Unit name	16-DC Input Unit (Source type)	
Type No.	PFJ-N161	
Rated input	24V DC	
Input voltage range	10V to 30V DC	
No. of inputs	16 points/unit (One common connection per 8 points)	
Input current	10mA/point (at 24V DC)	
Input impedance	2.3kΩ	
Input delay time	OFF → ON	7msec maximum
	ON → OFF	11msec maximum
Operating voltage	Minimum ON voltage	10V DC
	Maximum OFF voltage	3V DC
Input indication	LED indication	
Common polarity	Common terminal ..... (+)	
Internal current draw	40mA maximum	
Isolation method	Photocoupler	

Circuit configuration

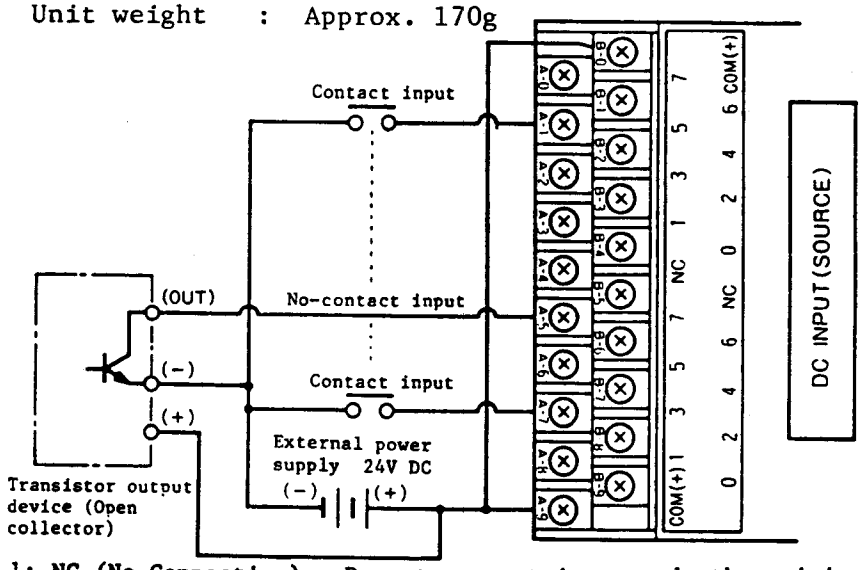


Note: External power supply is required for input.

External wiring example

Terminal screw: M3.5
Unit weight : Approx. 170g

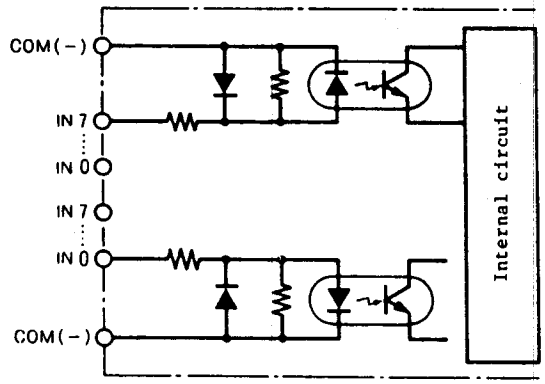
Terminal No.	Nameplate No.
B-0	COM(+)
A-0	7
B-1	6
A-1	5
B-2	4
A-2	3
B-3	2
A-3	1
B-4	0
A-5	7
B-6	6
A-6	5
B-7	4
A-7	3
B-8	2
A-8	1
B-9	0
A-9	COM(+)



Note 1: NC (No Connection) - Do not connect input and other wiring.
Note 2: Two COM (+) terminals are not connected together internally.

Unit name	16-DC Input Unit (Sink type)	
Type No.	PFJ-N162	
Rated input	24V DC	
Input voltage range	10V to 30V DC	
No. of inputs	16 points/unit (One common connection per 8 points)	
Input current	10mA/point (at 24V DC)	
Input impedance	2.3kΩ	
Input delay time	OFF → ON	7msec maximum
	ON → OFF	11msec maximum
Operating voltage	Minimum ON voltage	10V DC
	Maximum OFF voltage	3V DC
Input indication	LED indication	
Common polarity	Common terminal ..... (-)	
Internal current draw	40mA maximum	
Isolation method	Photocoupler	

Circuit configuration

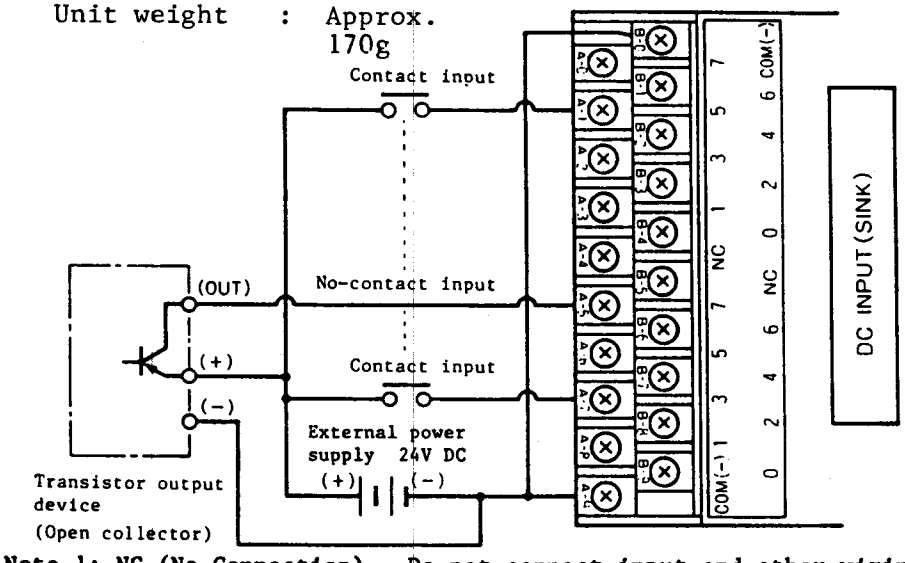


Note: External power supply is required for input.

External wiring example

Terminal screw: M3.5
Unit weight : Approx. 170g

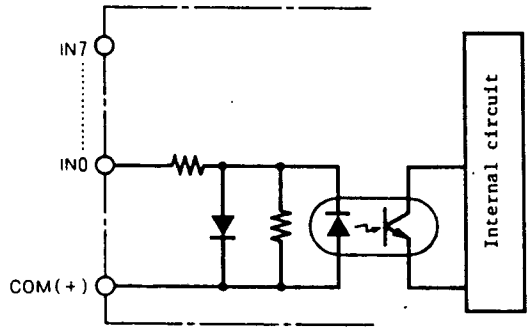
Terminal No.	Nameplate No.
B-0	COM(-)
A-0	7
B-1	6
A-1	5
B-2	4
A-2	3
B-3	2
A-3	1
B-4	0
A-5	7
B-6	6
A-6	5
B-7	4
A-7	3
B-8	2
A-8	1
B-9	0
A-9	COM(-)



Note 1: NC (No Connection) - Do not connect input and other wiring.
Note 2: Two COM (-) terminals are not connected together internally.

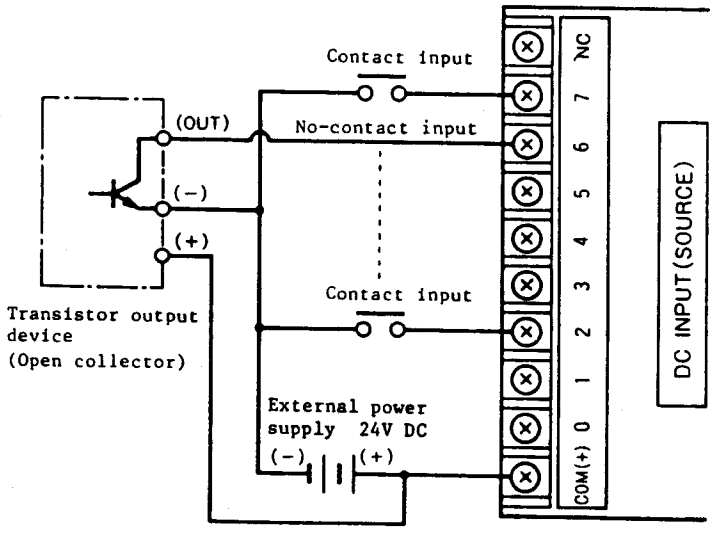
Unit name	8-DC Input Unit (Source type)	
Type No.	PFJ-N081	
Rated input	24V DC	
Input voltage range	10V to 30V DC	
No. of inputs	8 points/unit (One common connection per 8 points)	
Input current	10mA/point (at 24V DC)	
Input impedance	2.3kΩ	
Input delay time	OFF → ON	7msec maximum
	ON → OFF	11msec maximum
Operating voltage	Minimum ON voltage	10V DC
	Maximum OFF voltage	3V DC
Input indication	LED indication	
Common polarity	Common terminal ..... (+)	
Internal current draw	20mA maximum	
Isolation method	Photocoupler	

Circuit configuration



External wiring example

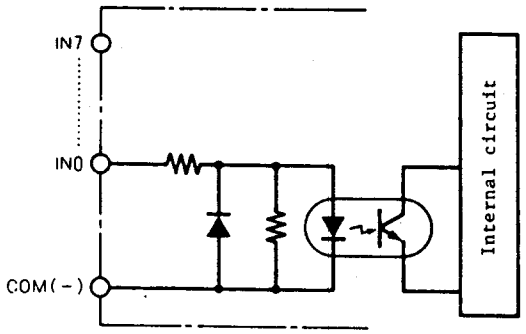
Terminal screw: M3.5
Unit weight : Approx. 120g



Note: NC (No Connection) - Do not connect input and other wiring.

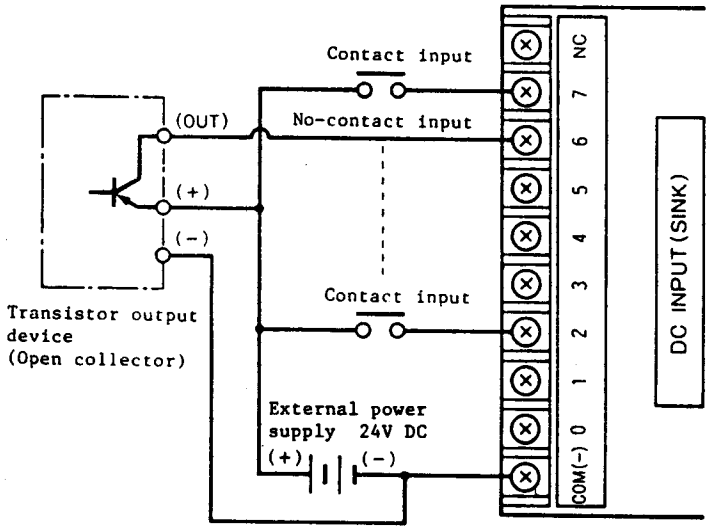
Unit name	8-DC Input Unit (Sink type)		
Type No.	PFJ-N082		
Rated input	24V DC		
Input voltage range	10V to 30V DC		
No. of inputs	8 points/unit (One common connection per 8 points)		
Input current	10mA/point (at 24V DC)		
Input impedance	2.3kΩ		
Input delay time	OFF → ON	7msec maximum	
	ON → OFF	11msec maximum	
Operating voltage	Minimum ON voltage	10V DC	
	Maximum OFF voltage	3V DC	
Input indication	LED indication		
Common polarity	Common terminal ..... (-)		
Internal current draw	20mA maximum		
Isolation method	Photocoupler		

Circuit configuration



External wiring example

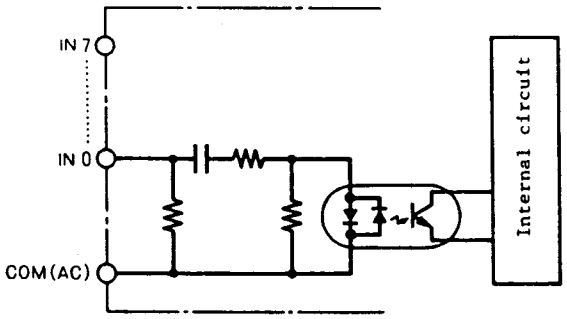
Terminal screw: M3.5
Unit weight : Approx. 120g



Note: NC (No Connection) - Do not connect input and other wiring.

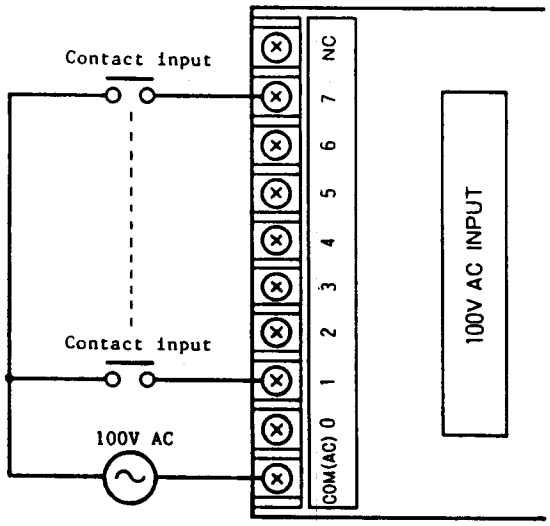
Unit name	8-100V AC Input Unit		
Type No.	PFJ-N083		
Rated input	100V to 120V AC		
Input voltage range	85V to 132V AC		
No. of inputs	8 points/unit (One common connection per 8 points)		
Input current	9mA/point (at 100V AC)		
Input impedance	12kΩ		
Input delay time	OFF → ON	65msec maximum (at 100V AC)	
	ON → OFF	80msec maximum (at 100V AC)	
Operating voltage	Minimum ON voltage	60V	
	Maximum OFF voltage	30V	
Input indication	LED indication		
Internal current draw	8mA maximum		
Isolation method	Photocoupler		

Circuit configuration



External wiring example

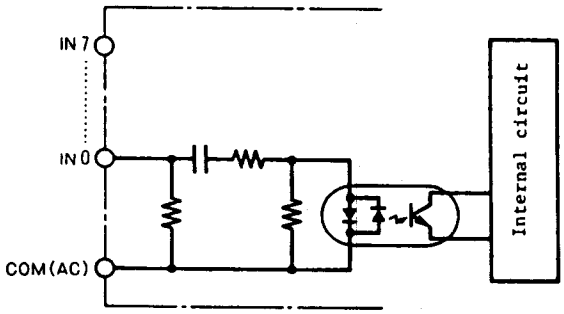
Terminal screw: M3.5
Unit weight : Approx. 150g



Note: NC (No Connection) - Do not connect input and other wiring.

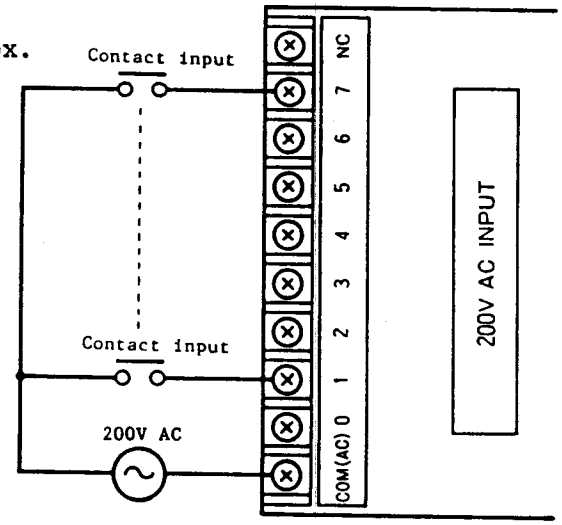
Unit name	8-200V AC Input Unit		
Type No.	PFJ-N084		
Rated input	200V to 240V AC		
Input voltage range	170V to 264V AC		
No. of inputs	8 points/unit (One common connection per 8 points)		
Input current	8mA/point (at 200V AC)		
Input impedance	28kΩ		
Input delay time	OFF → ON	66msec maximum (at 200V AC)	
	ON → OFF	80msec maximum (at 200V AC)	
Operating voltage	Minimum ON voltage	120V	
	Maximum OFF voltage	60V	
Input indication	LED indication		
Internal current draw	8mA maximum		
Isolation method	Photocoupler		

Circuit configuration



External wiring example

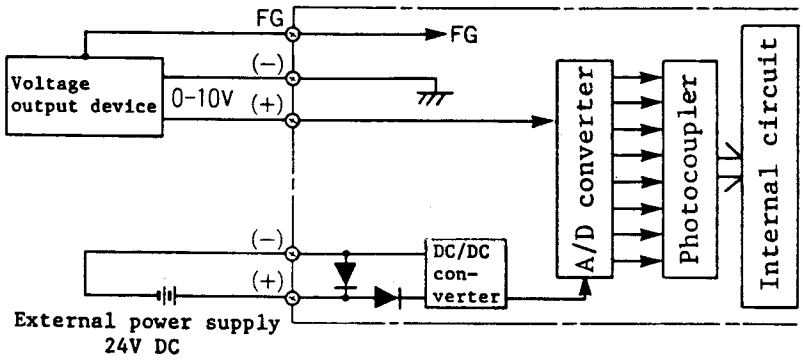
Terminal screw: M3.5
Unit weight : Approx. 150g



Note: NC (No Connection) - Do not connect input and other wiring.

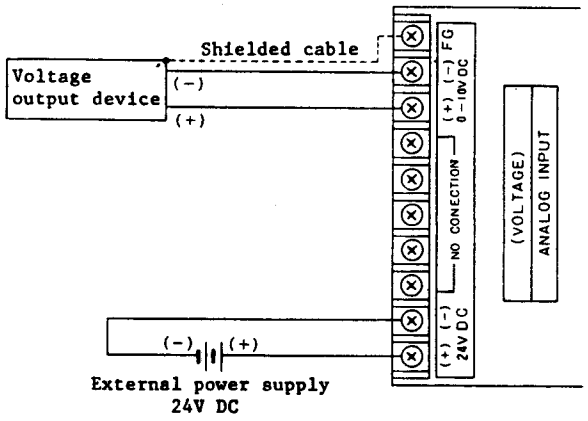
Unit name	Analog Input Unit (Voltage Input Type)
Type No.	PFJ-N012
Input voltage range	0 to 10V DC
Input impedance	20kΩ
No. of input	1 (occupies 8 input points)
Input characteristics	Analog value (Input) / Digital value 9.961V / 255 7.813V / 200 5.000V / 128 3.906V / 100 1.953V / 50 0 V / 0 (Rounded to 3 decimals)
Resolution	8 bits, 10/256 (Approx. 39mV)
Total accuracy	±1% maximum (of the full scale)
Maximum input	+12V, -0.2V
External power supply	Voltage: 24V DC (±10%) Current draw: 60mA maximum
Internal current draw	5mA maximum
Isolation method	Photocoupler
Input response	2 scan time maximum

Circuit configuration



External wiring example

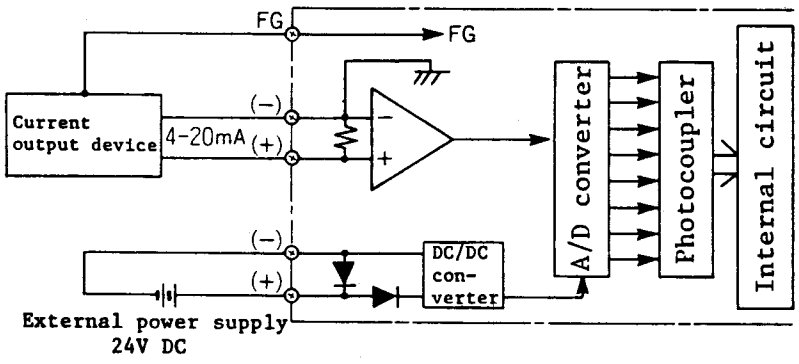
Terminal screw: M3.5
Unit weight : Approx. 165g



Note: NO CONNECTION Terminals - Do not connect input and other wiring.

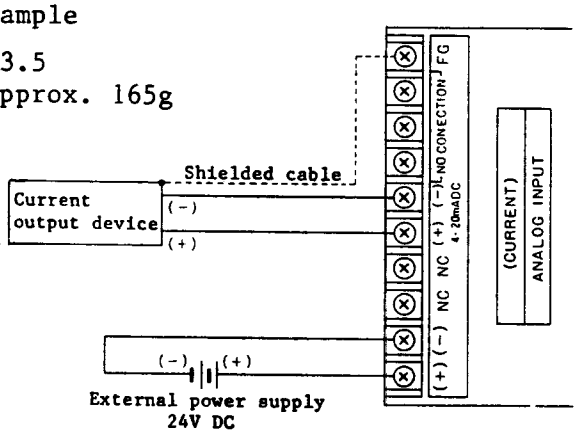
Unit name	Analog Input Unit (Current Input Type)	
Type No.	PFJ-N013	
Input current range	4 to 20mA DC	
Input impedance	250Ω	
No. of input	1 (occupies 8 input points)	
Input characteristics	Analog value (Input)	Digital value
	19.938mA	255
	16.500mA	200
	12.000mA	128
	10.250mA	100
	7.125mA	50
	4 mA	0
	(Rounded to 3 decimals)	
Resolution	8 bits, 16/256 (Approx. 0.063mV)	
Total accuracy	±1% maximum (of the full scale)	
Maximum input	23mA	
External power supply	Voltage: 24V DC (±10%) Current draw: 60mA maximum	
Internal current draw	5mA maximum	
Isolation method	Photocoupler	
Input response	2 scan time maximum	

Circuit configuration



External wiring example

Terminal screw: M3.5
Unit weight : Approx. 165g

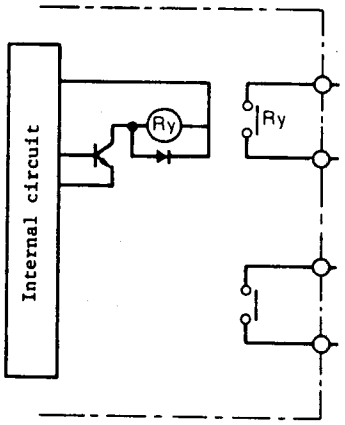


Note: NO CONNECTION Terminals - Do not connect input and other wiring.

Output Specifications

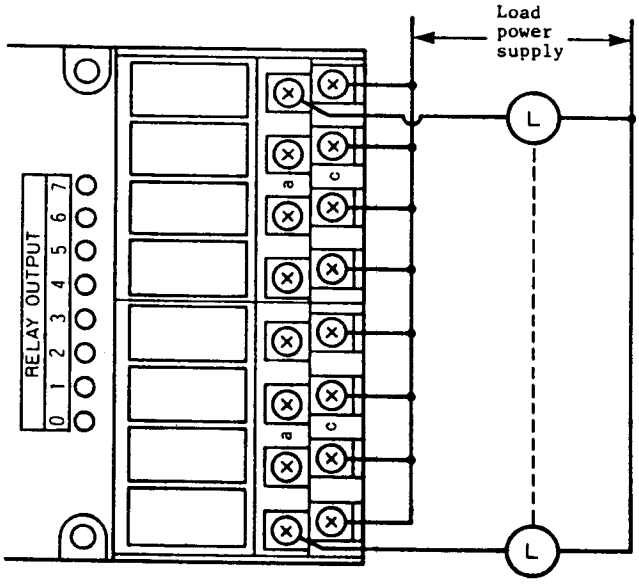
Unit name	8-Relay Output Unit
Type No.	PFJ-T081
No. of outputs	8 points/unit
Output signal	Relay output, Independent 1NO, Relay can be replaced. 110V AC, 5A (220V AC, 2A) cos ø = 1 (Each module can be replaced with a transistor or SSR output module.)
Output indication	LED indication
Internal current draw	150mA
Other specifications	For specifications of RS1S output relay and each module, refer to Specifications and Wiring.

Circuit configuration



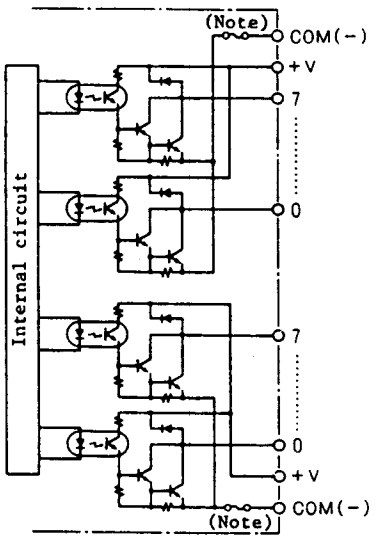
External wiring example

Terminal screw: M3.5
Unit weight : Approx. 250g



Unit name	16-Transistor Output Unit	
Type No.	PFJ-T162	
Output mode	Transistor output	
No. of outputs	16 points/unit (One common connection per 8 points)	
Rated load voltage	12V to 28V DC ±10%	
Max. load current	0.5A/circuit (2.5A/common connection)	
Max. rush current	8A	
Max. leakage current	100μA	
Isolation method	Photocoupler	
Delay time	OFF → ON	1msec maximum
	ON → OFF	1msec maximum
ON voltage	1.5V maximum	
External current draw	12V to 28V DC 30mA	
Output indication	LED indication	
Internal current draw	40mA maximum	

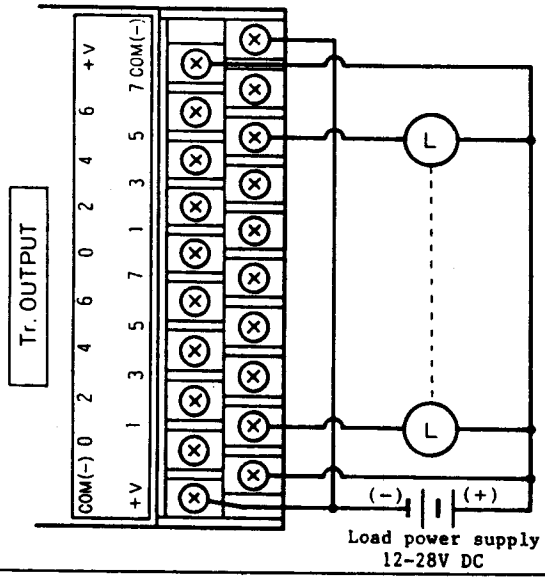
Circuit configuration



Note: Internal fuse (8A)

External wiring example

Term. No.	Nameplate No.
B-0	COM(-)
A-0	+V
B-1	0
A-1	1
B-2	2
A-2	3
B-3	4
A-3	5
B-4	6
A-4	7
B-5	0
A-5	1
B-6	2
A-6	3
B-7	4
A-7	5
B-8	6
A-8	7
B-9	+V
A-9	COM(-)



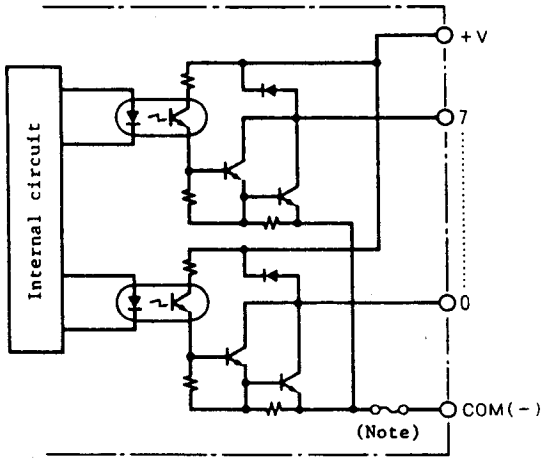
Terminal screw: M3.5

Unit weight: Approx. 200g

Note:
Two COM(-) terminals and two +V terminals are not connected together internally.

Unit name	8-Transistor Output Unit	
Type No.	PFJ-T082	
Output mode	Transistor output	
No. of outputs	8 points/unit (One common connection per 8 points)	
Rated load voltage	12V to 48V DC ±10%	
Max. load current	1.0A/circuit (4.0A/common connection)	
Max. rush current	5A	
Max. leakage current	100μA	
Diode for fly-back voltage absorption	Diode reverse voltage: 110V Diode forward current: 5A	
Isolation method	Photocoupler	
Delay time	OFF → ON	1msec maximum
	ON → OFF	1msec maximum
ON voltage	1.5V maximum	
External current draw	12V to 48V DC 40mA maximum	
Output indication	LED indication	
Internal current draw	25mA maximum	

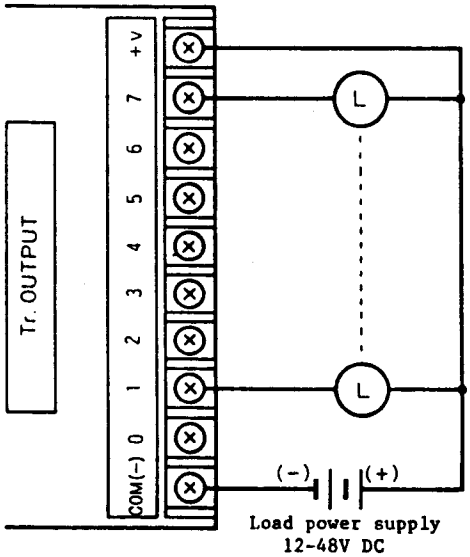
Circuit configuration



Note: Internal fuse (8A)

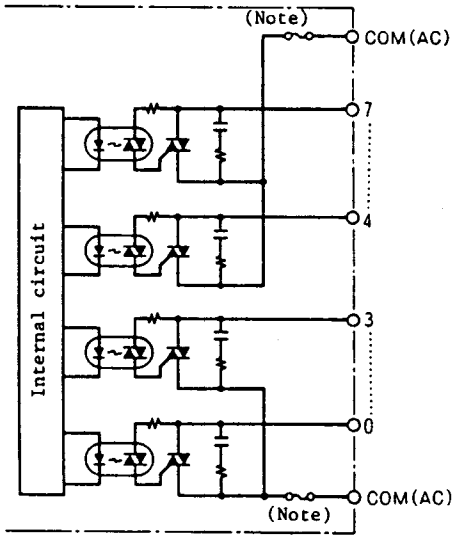
External wiring example

Terminal screw: M3.5
Unit weight : Approx. 170g



Unit name	8-SSR Output Unit	
Type No.	PFJ-T083	
Output mode	Triac output (without zero-switching function)	
No. of outputs	8 points (One common connection per 4 points)	
Rated load voltage	100V to 240V AC, +10% to -15%	
Max. load current	1.0A (2.0A/common connection)	
Max. rush current	1-cycle surge current 20 Arms	
Max. leakage current	Max. 6.0mA rms (240V AC)	
Min. load current	Min. operating current 20mA	
Isolation method	Photocoupler	
Delay time	OFF → ON	1msec maximum
	ON → OFF	1/2 cycle +1msec maximum
Output indication	LED indication	
Internal current draw	130mA maximum	

Circuit configuration

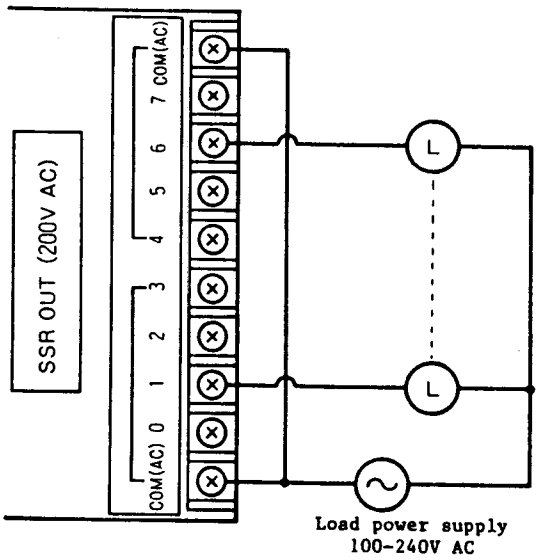


Note: Internal fuse (6A)

External wiring example

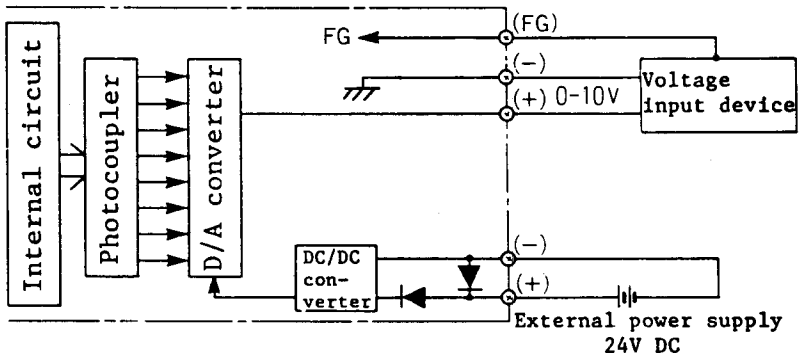
Terminal screw: M3.5
Unit weight : Approx. 210g

Note: Two COM (AC) terminals are not connected together internally.



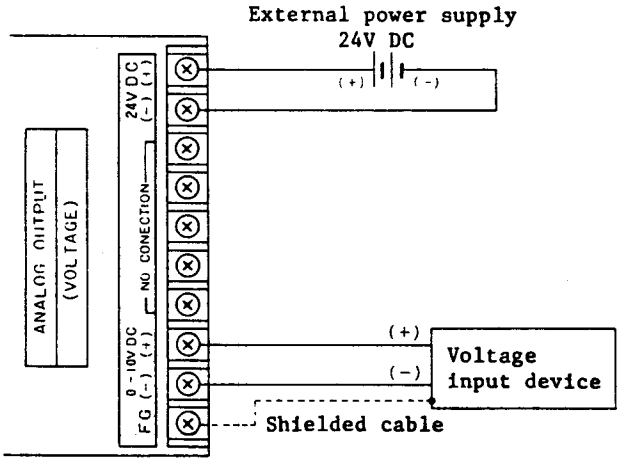
Unit name	Analog Output Unit (Voltage Output Type)
Type No.	PFJ-T012
Output voltage range	0 to 10V DC
Allowable load impedance	10kΩ minimum
No. of output	1
Output characteristics	Digital value / Analog value (Output) 255 / 9.961V 200 / 7.813V 128 / 5.000V 100 / 3.906V 50 / 1.953V 0 / 0 V (Rounded to 3 decimals)
Resolution	8 bits (39mV)
Total accuracy	±1% maximum (of the full scale)
Maximum output	Approx. 9.961V
External power supply	Voltage: 24V DC (±10%) Current draw: 70mA maximum
Internal current draw	14.5mA maximum
Isolation method	Photocoupler
Output response	1 msec maximum

Circuit configuration



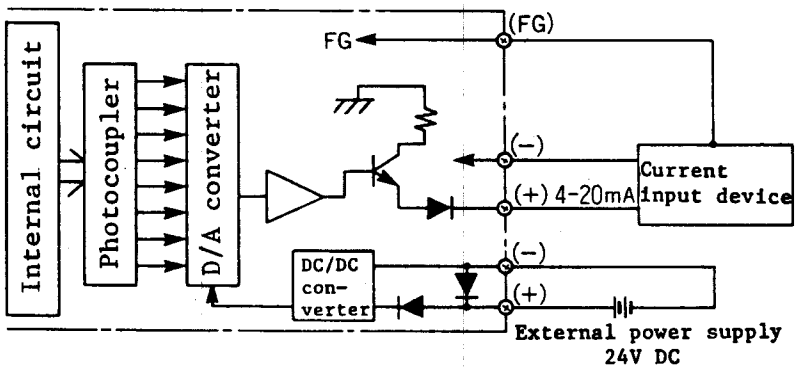
External wiring example

Terminal screw: M3.5
Unit weight : Approx. 155g



Unit name	Analog Output Unit (Current Output Type)	
Type No.	PFJ-T013	
Output current range	4 to 20mA DC	
Allowable load impedance	270Ω maximum	
No. of output	1	
Output characteristics	Digital value	Analog value (Output)
	255	19.938mA
	200	16.500mA
	128	12.000mA
	100	10.250mA
	50	7.125mA
	0	4.000mA
	(Rounded to 3 decimals)	
Resolution	8 bits (0.063mA)	
Total accuracy	±1% maximum (of the full scale)	
Maximum output	Approx. 19.94mA	
External power supply	Voltage: 24V DC (±10%) Current draw: 70mA maximum	
Internal current draw	14.5mA maximum	
Isolation method	Photocoupler	
Output response	1 msec maximum	

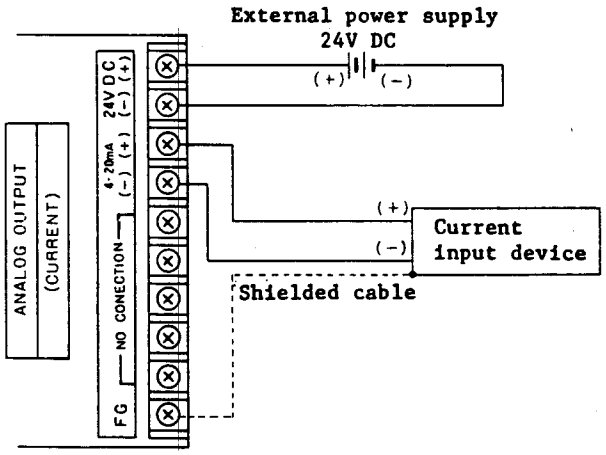
Circuit configuration



External wiring example

Terminal screw: M3.5

Unit weight : Approx. 155g

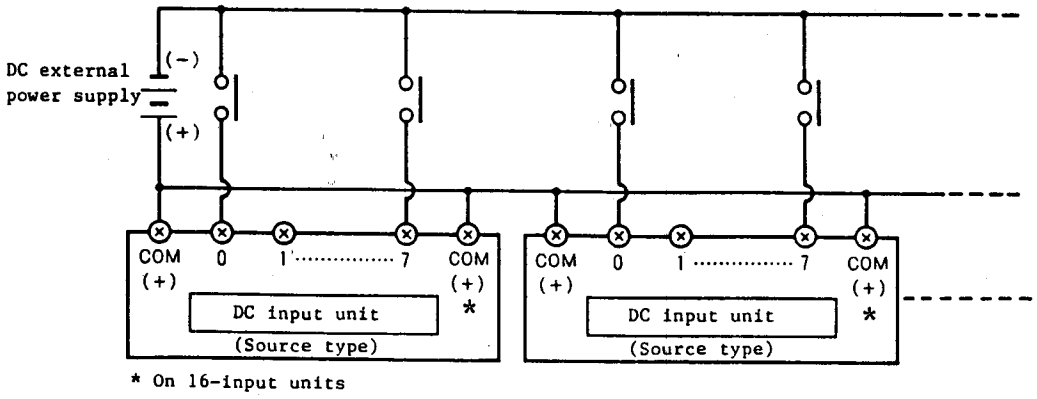


Note: NO CONNECTION Terminals - Do not connect input and other wiring.

Wiring for Input Units

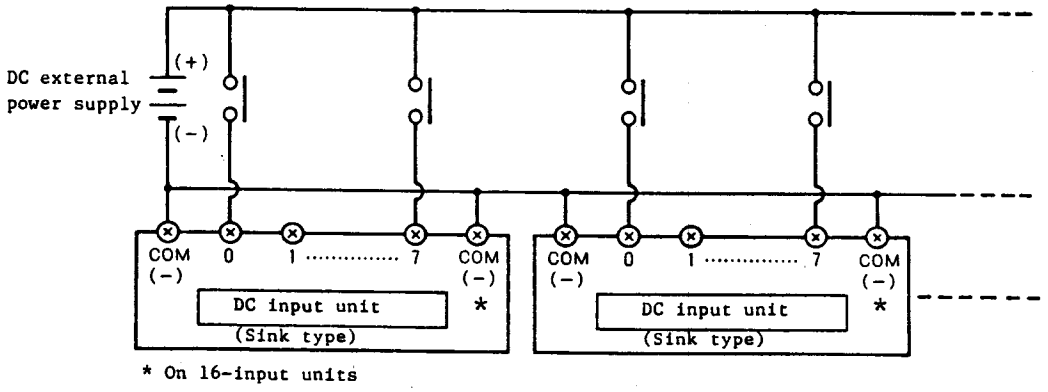
Note: Be sure to avoid contact between COM (+), COM (-) and COM (AC) of input units.

- **When two or more 8- or 16-DC input units (source type) are used**



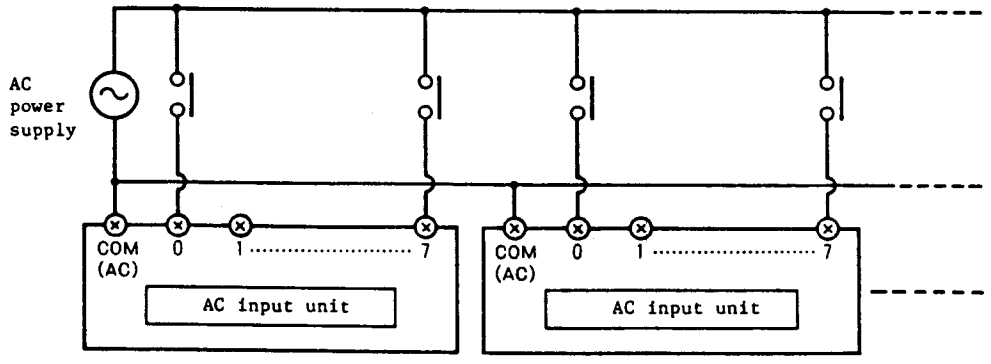
* On 16-input units

- **When two or more 8- or 16-DC input units (sink type) are used**



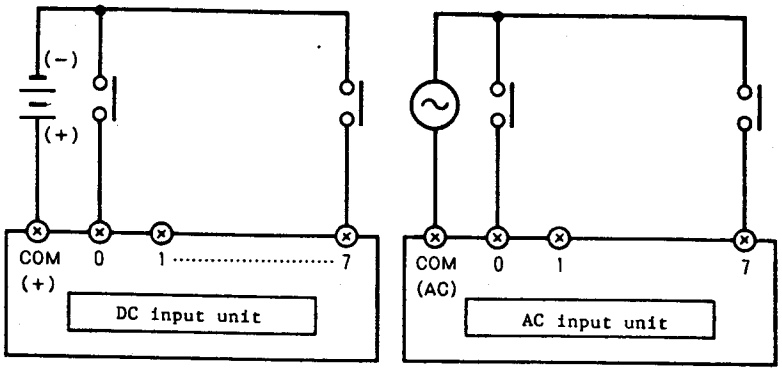
* On 16-input units

- **When two or more AC input units are used**



- **When DC input unit and AC input unit are used in combination**

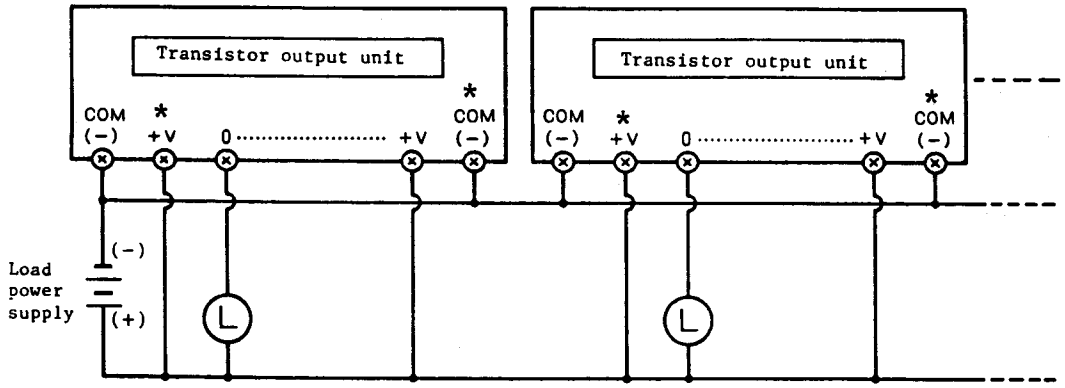
  Be sure to avoid contact between DC and AC input wiring.



Note: Be sure to avoid contact between COM (+), COM (−) and COM (AC) of input units.

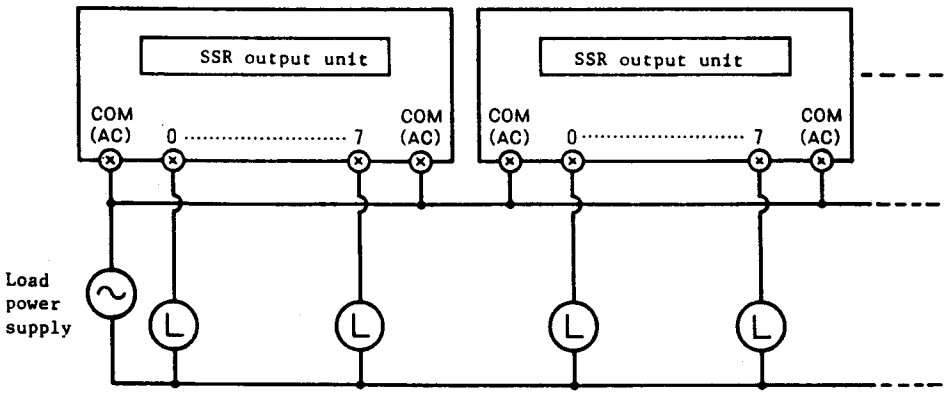
Wiring for Output Units

- **When two or more transistor output units are used**



* On 16-output units

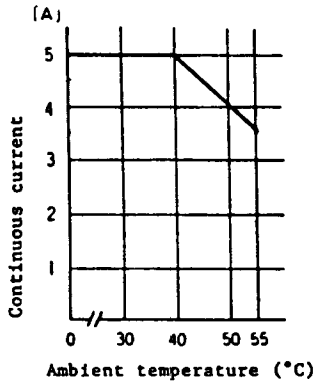
- **When two or more SSR output units are used**



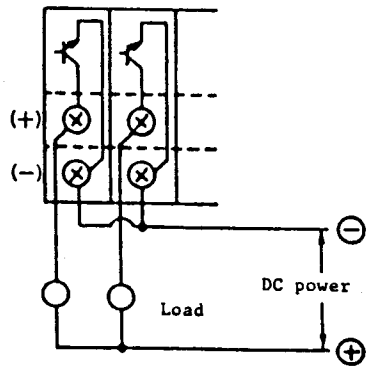
Mechanical Contact Output Relay (Type RS1S-5A)

Contact configuration	1NO
Rated load	Resistive load: 110V AC 5A 220V AC 2A 24V DC 5A Inductive load: 110V AC 2A (cos ø = 0.4) 220V AC 1A (cos ø = 0.4) 24V DC 2A (L/R = 7msec)
Maximum switching & continuous current	5A
Maximum switching voltage	250V AC, 60V DC
Maximum switching capacity	Resistive load: AC: 550VA, DC: 120W Inductive load: AC: 220VA (cos ø = 0.4) DC: 48W (L/R = 7msec)
Minimum applicable load	5V DC 1mA (reference value)
Contact resistance	50mΩ maximum (initial value)
Operate time	15msec maximum including bounce (at the rated voltage)
Mechanical life (No-load)	50,000,000 operations or more (at 18,000 operations/hr)
Electrical life (Rated load)	200,000 operations or more (at 1,800 operations/hr)

Continuous Current-Ambient Temperature Characteristics



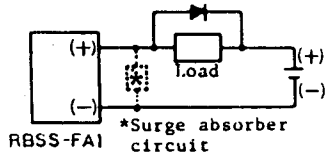
Transistor Output Module (Type RBSS-FA1)

Load voltage	24V DC
Power supply frequency	——
Max. load current	0.4A
Load voltage range	10V to 28V DC
OFF-state leakage current	0.1mA maximum
Min. operating current	1mA (Resistive load)*1
Contact voltage drop	1V maximum
Surge current (Absolute maximum load voltage)	2A (1 sec) maximum (30V DC)
Operate time	0.1msec maximum (R load)
Release time	0.2msec (Typ.) (R load)
Wiring diagram	

*1 When non-resistive loads are used, operate this module at 10mA or more.

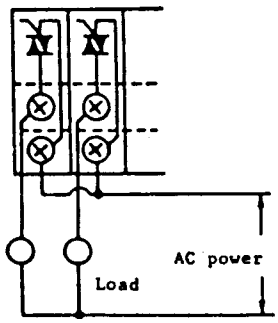
Precautions for operating transistor output modules

- Take care so that the load voltage and current do not exceed the rated values.
- The rated load voltage is a value at DC without ripple.
- When a small capacity load is connected, the load may fail to reset due to a leakage current even if the transistor is turned OFF. In this case, connect a resistor in parallel with the load and shunt the leakage current.
- It should be noted that the transistor may sometimes be damaged if power is reversely connected to the output terminal.
- When driving an inductive load, be sure to connect a diode across the load to absorb a counter electromotive force.



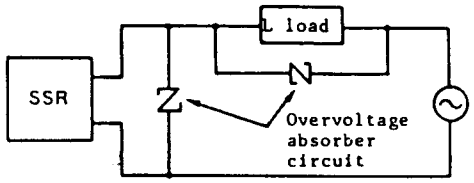
- When the transistor output side terminal is subjected to a noise voltage exceeding the rated voltage, connect a varistor to the output terminals in order to absorb the overvoltage.

SSR Output Module (Type RASS-FA1)

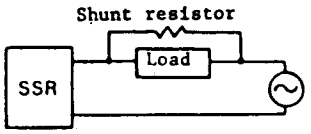
Load voltage	200V AC
Power supply frequency	50/60Hz
Max. load current	0.2A
Load voltage range	70V to 250V AC
OFF-state leakage current	1mA (100V AC) 2mA (200V AC)
Min. operating current	20mA
Contact voltage drop	3V rms maximum
Surge current	8A peak (non-repetitive)
Operate time	1msec maximum
Release time	1/2 cycle + 1msec maximum
Wiring diagram	

Precautions for operating SSR output modules

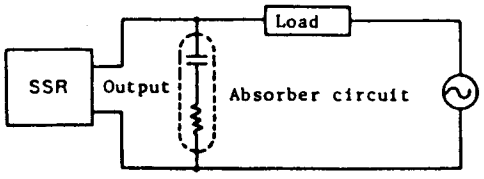
- Special care should be given so that the circuit voltage and current do not exceed the rated values. Avoid using this module where abnormal surge voltage takes place.
- If SSR wiring run in parallel with power lines, induction may cause maloperation: separate these wires as far apart as possible.
- When an inductive load is switched, or in the presence of external noise, connect overvoltage absorbing elements to both ends of the load and the output terminals of the SSR.



- When a small capacity load is connected, the load may fail to reset due to a leakage current even if the SSR is turned OFF. In this case, connect a resistor in parallel with the load to shunt the leakage current.



- The SSR output module does not contain a surge absorber circuit: always connect an RC absorber to the output terminals.



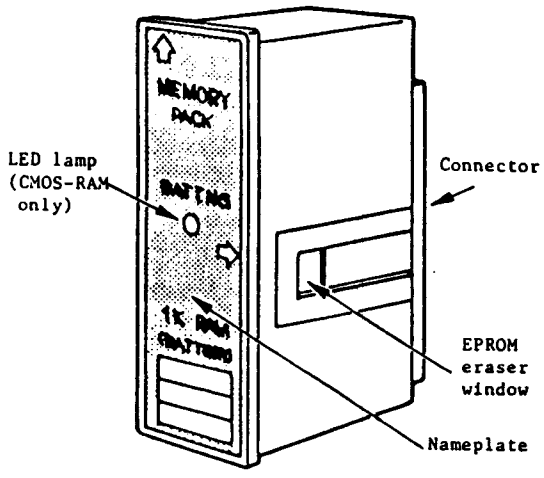
C: 0.1μF 600WV (Film capacitor)
R: 100Ω ½W

C: 0.047μF 600WV (Film capacitor)
R: 22Ω ½W

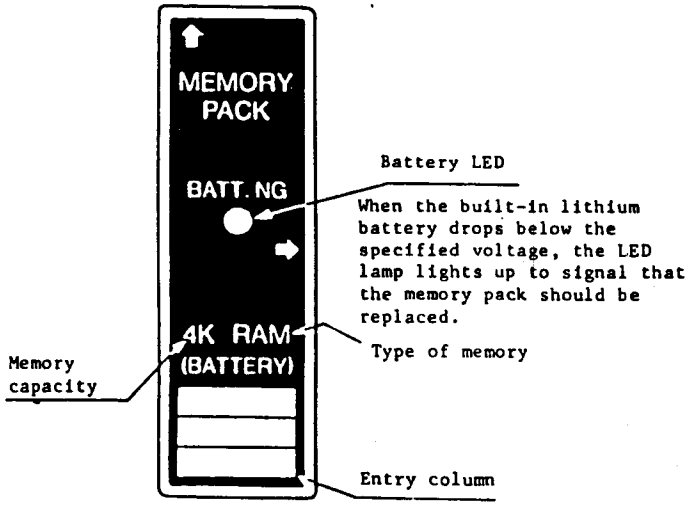
Type and Application of the Memory Pack

- Hints on memory pack selection

Type	Type No.	Memory Features	Name-plate Color
CMOS-RAM (with battery)	• For 1K steps PFA-1M21 • For 4K steps PFA-1M24	Programs can be optionally written and read. Most suitable for programs modified often and system startup. Effective memory period is 5 years. When programs must be stored over 5 years, use an E^2PROM or EPROM.	Green
E^2PROM	• For 4K steps PFA-1M14	Read only memory. A program loader can only be used to erase all data electrically and to rewrite data. Most suitable for normal operation after system startup.	Blue
EPROM	• For 4K steps PFA-1M34	Read only memory. Programs can be written using a program loader but cannot be modified or erased. Most suited for massproduced equipment whose programs are fixed.	Brown



(1) CMOS-RAM memory pack
(Lithium battery built-in)



- CMOS-RAM pack replacement procedures

① After placing the CPU unit in the stop condition, connect the program loader to the CPU unit.

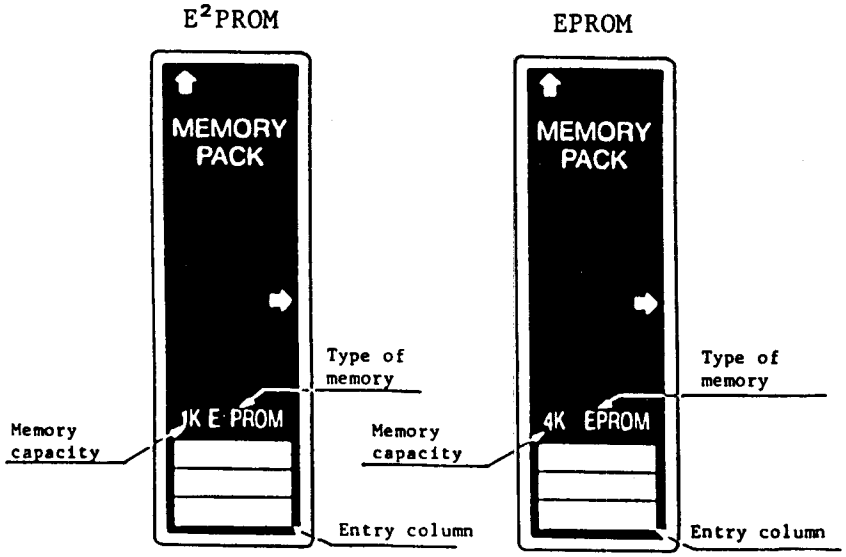
② After the transferring (read) operation ("TRS", "READ" and "ENTR"), transfer the program within the CMOS-RAM pack to the program loader.

③ Replace the old CMOS-RAM pack with a new one.

④ By the transferring (write) operation ("TRS", "ENTR" and "ENTR"), transfer the program within the program loader to the CMOS-RAM pack.

⑤ Re-start operation.

(2) E^2PROM, EPROM memory pack



Note: To erase the EPROM memory pack, a special PROM eraser is required.

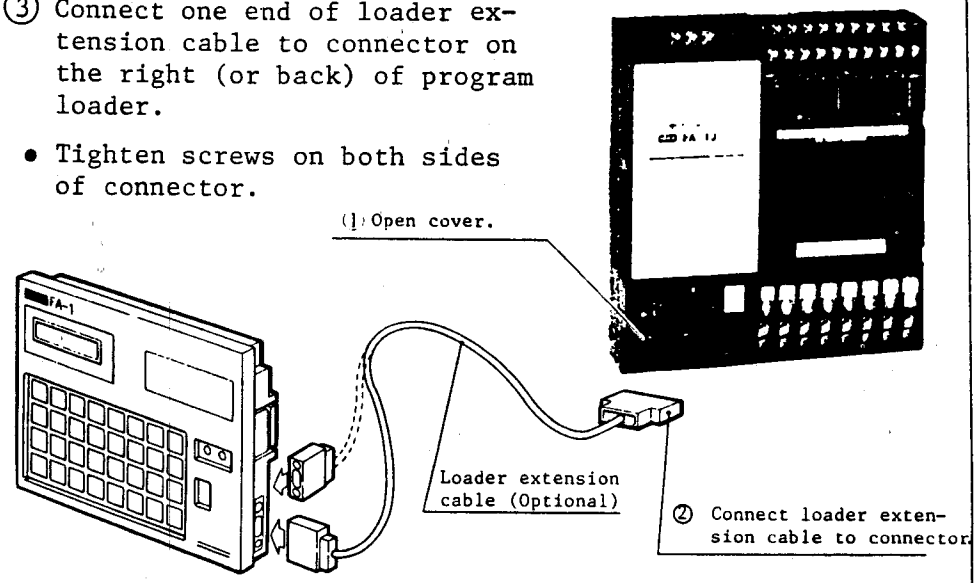
Basic Operation

(1) Connection between CPU unit and program loader

A loader extension cable (Type No. PFA-1A11) is necessary for connection.

③ Connect one end of loader extension cable to connector on the right (or back) of program loader.

- Tighten screws on both sides of connector.

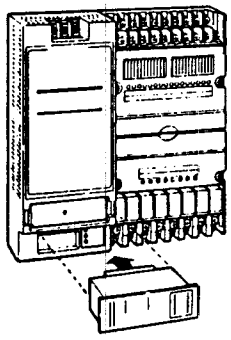


(2) Removing and re-installing memory pack

Memory pack, can be installed on the CPU unit and the program loader.

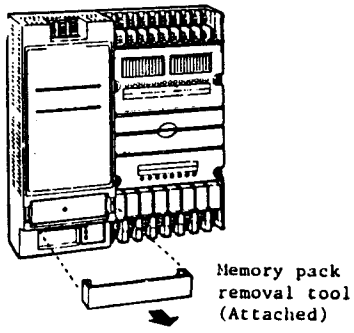
(A) Removal from and re-installation to the CPU unit

(Memory pack insertion)



- Insert the memory pack into the connector on the left side of the CPU unit, and push it to its full depth.

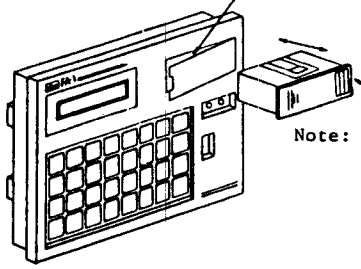
(Memory pack removal)



- Fit the memory pack removal tool into the right and left parts of the memory pack as illustrated and pull it toward you.

Note: When removing or re-installing the CMOS-RAM memory pack, please note that the contents of the memory may be erased. When writing a program from the loader to the RAM pack, be sure to mount the RAM pack to the CPU unit.

(B) Program loader removal and re-installation



Note: Only the E^2PROM and EPROM memory packs can be removed from and re-installed to the program loader. If the RAM pack is removed or re-installed, the contents of the memory may be erased.

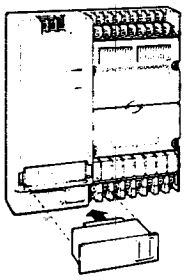
Procedure before Starting Operation

There are two different procedures for operations between programming and starting operation according to the memory packs.

CMOS-RAM Memory Pack

1 Mount the memory pack into the CPU unit.

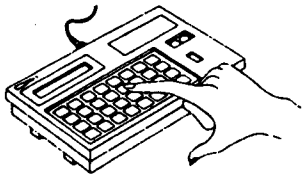
Load the CMOS-RAM memory pack into the CPU unit.



2 Turn power ON.

3 Start programming.

Use the program loader for programming.



4 Transferring

After connecting the program loader to the CPU unit, transfer the program from the program loader to the CMOS-RAM pack on the CPU unit.

Note: Transferring operation must be carried out after stopping the CPU unit operation.

5 Start operation.

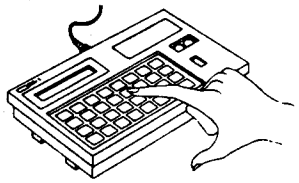
Before starting operation, remember to clear all errors.
Upon completion of program transferring, start operation. (See the next page.)

E^2PROM or EPROM Memory Pack

1 Turn power ON.

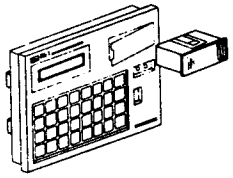
2 Start programming.

Use the program loader for programming.



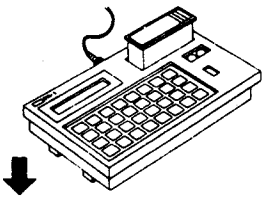
3 Mount the memory pack into the loader.

Mount an E^2PROM or EPROM memory pack into the loader.



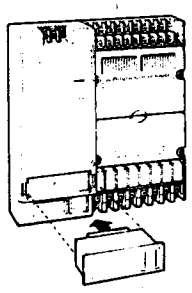
4 PROM writing operation

Use the program loader for PROM writing operations.



5 Mount the memory pack into the CPU unit.

Mount E^2PROM or EPROM memory pack to the CPU unit.



6 Start operation.

Before starting operation, be sure to clear all errors. (For operation, see the next page.)

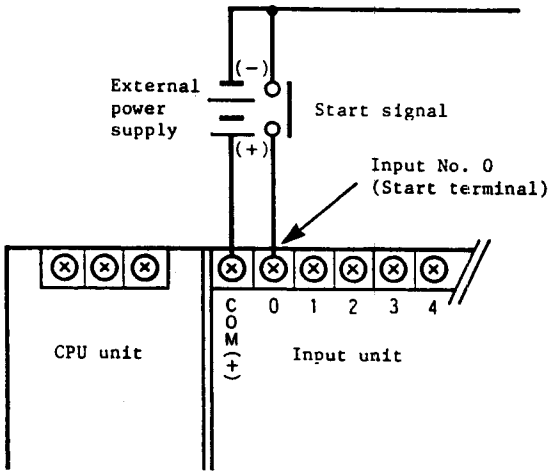
Note: In a system using an E^2PROM, use a RAM memory pack when the system is started up: this can reduce the time required for transferring the program.

FA-1J start and stop operations include: 1) start/stop operation via start signal, 2) automatic start/stop operation via power supply and 3) start/stop operation via special internal relay. Input No. 0 can be designated as a start terminal, and any input number can be designated as a stop or reset terminal using the function (FUN) key, thus providing control inputs. (Exclusive start, stop and reset terminals are not provided.)

Start

(1) Start/stop operation via start signal

- Input No. 0 is designated as start terminal.

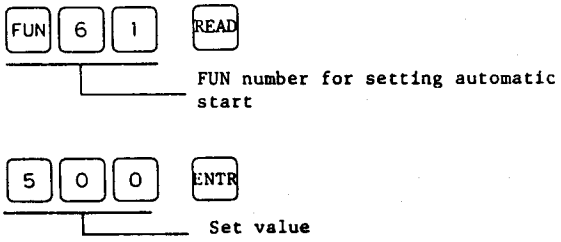


- The start input works as start and stop inputs: when the start input is turned ON, operation starts ("RUN" lamp lights), and when it is OFF, operation stops ("RUN" lamp goes off).
- The start input allows the edge (level) start: even when power is turned ON after the start input is ON, operation is started.

Automatic Start/Stop Operation via Power Supply

(2) Automatic start/stop operation via power supply

- When FUN61 is set to 500, the start function of Input No. 0 is released, and this number can be used as an ordinary input.



500: Automatic start function
0: Automatic start function release

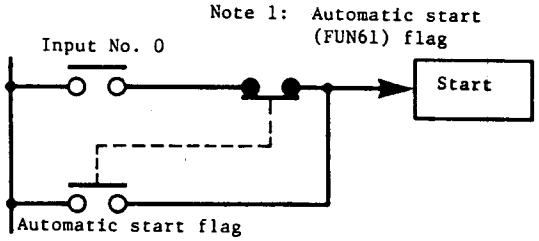
The value 0 is set when program all-clear operation is performed.

Note 1: If values other than 500 and 0 are set, they will be written into the program loader and memory pack, but operation will not start upon turning on FA-IJ power (the ERROR lamp will light).

Note 2: Since the setting is written into the memory pack, the setting must be performed prior to transferring the program.

Supplement 1

The start operation functions (1) and (2) are illustrated as follows:



Note 1: Automatic start flag

- When FUN61 is set to 500 ... ON
- When FUN61 is set to 0 ... OFF

(3) Start/stop operation via special internal relay

- When start input of Input No. 0 is turned on, or when automatic start is designated by setting FUN61 to 500, the FA-1J starts upon turning on special internal relay 701 firstly, and then 702, and stops upon turning them off.

Special IR 701	OFF			Without start function via special IR
	ON	Special IR 702	OFF	FA-1J operation stop
			ON	FA-1J operation start

- Start/stop operation can be performed by turning special internal relays 701 and 702 on or off directly from program loader via the SET and RST keys, using this function. This operation is convenient in starting up the system. Also, start/stop operation from personal computer is possible.

Note: Internal relay 701 can be set by pressing:

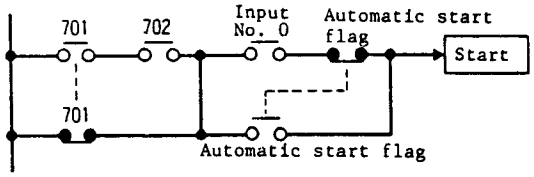
[TRS] [SET] [7] [0] [1] [ENTR]

Internal relay 702 can be reset by pressing:

[TRS] [RST] [7] [0] [2] [ENTR]

Supplement 2

Start operation functions explained in (1), (2) and (3) are illustrated as follows:



Note 1: A system equivalent to this circuit is programmed in the FA-1J system program.

Note 2: If stop input is designated by FUN4, start/stop operation as shown above cannot be performed by internal special relays 701 and 702.

Important

Since the program is checked after the start input is turned on, the following time is required until RUN is made (RUN lamp lights).

1K steps: Approx. 1 sec
4K steps: Approx. 4 sec

Stop & Reset

- For systems requiring stop and reset inputs, any input number can be designated via FUN. (For the setting method, see "Program Loader Operating Procedures (FUN4 and 5)".)
- When stop or reset input is turned on during operation, the RUN lamp goes off and operation stops. (All outputs are turned off.)
- When only reset input is set, start input remains as a start/stop input (continuous signal).
- When stop input is set, start signal input (Input No. 0) can accept one-shot input.
- The priority of signals is: reset → stop → start input. Reset input has precedence over the others.

Supplement 3

Data status in start, stop and reset modes.

	Output	IR/SFR Status, CNT Counted Value		Timer Counted Value	CNT 45 & 46 Counted Value
		Keep Setting Area during Power Failure	Non-holding Area during Power Failure		
Starting	Operating	Operating	Operating	Operating	Operating
Resetting	Off	Clear	Clear	Unchanged	Unchanged
Stopping	Off	Unchanged	Unchanged	Unchanged	Unchanged
At start (Instantaneous)	Unchanged	Unchanged	Clear	Clear (Initialize)	Unchanged

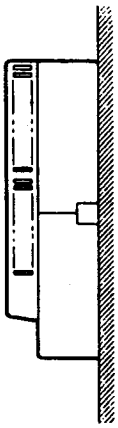
Installation and wiring operations should be carried out with due consideration taken for operating convenience, maintainability and resistance to the environment so that the FA-1J can perform at full capacity.

Installation Location

(1) Avoid installing the unit in the following locations.

① Where ambient temperature drops below 0°C or exceeds +55°C;
② Where ambient humidity drops below 45% or exceeds 85% RH;
③ Where the unit is exposed to large amounts of dust or dirt, salt, iron powder, etc.;
④ Where the unit is exposed to direct sunlight;
⑤ Where the unit is subject to vibrations or shocks; and
⑥ Where corrosive or flammable gas is present.

(2) To install the FA-1J, reserve a sufficient space away from the surrounding fixture, heating element and panel for better ventilation. Always install the unit on a vertical surface as illustrated below.

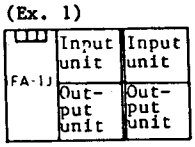


Input/Output Unit Expansion

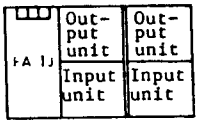
(1) Input/output unit installation position

① Two input or output units can be loaded on one CPU unit. For expansion, connect base units (two input or output units can be loaded on one base unit) via extension cable.
② Though input/output units can be loaded on both upper and lower part, it is recommended to load input units on the upper part and output units on the lower part. By so doing, input and output lines can be separated at wiring.

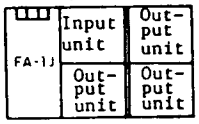
(Ex. 1)



(Ex. 2)



(Ex. 3)

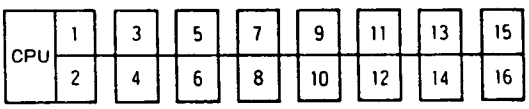


Supplement (Spare Label)

Labels of input and output units are attached for installation on upper and lower parts respectively at shipment. When they are installed conversely, remove the labels and attach spare labels.

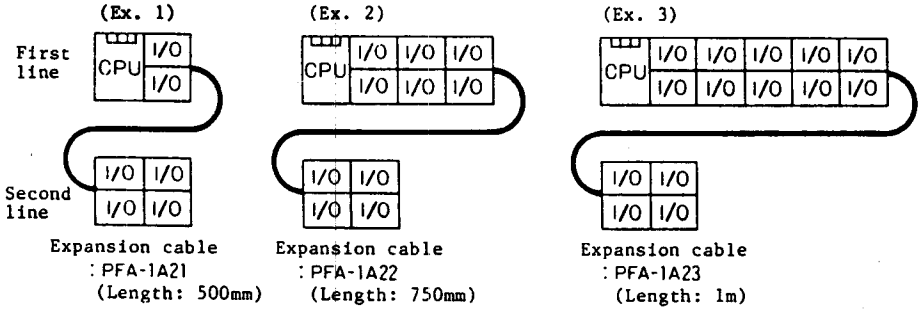
③ Load dummy units to fill the void in base unit. If the void remains unfilled, signals are not sent to input or output units beyond the void, because they are sent in the order of the number shown below.

Note: When the void exists in the last number, dummy units are not required functionally, but better be used for protecting the connector.



FA-1J Expansion by One Line or More

When FA-1J is expanded by one line or more due to limited installation space, use an I/O expansion cable.



Note: Fix the I/O expansion cable on a mounting plate; instead of installing it in a wiring conduit.

(2) Use of expansion power supply unit

① The CPU unit has a built-in power supply for driving input and output units, but the number of applicable input and output units is limited. As internal current draw varies with units, calculate the number from the list below. When power capacity is insufficient, use an expansion power supply unit. (These power supplies cannot be used as an external power supply for DC input units.)

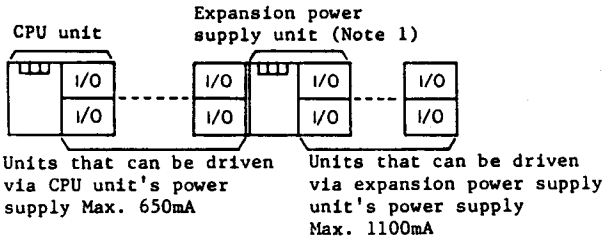
② Power capacity that can be provided

Unit Name	Power Supply Capacity
CPU unit	650mA
Expansion power supply unit	1100mA

③ Internal power consumption

Unit Name	Internal Current Draw
DC 16-input unit	40mA
DC 8-input unit	20mA
100V AC input unit	8mA
200V AC input unit	8mA
Relay output unit	150mA
Transistor 16-output unit	40mA
Transistor 8-output unit	25mA
SSR output unit	130mA
Analog input unit	5mA
Analog output unit	15mA

The above values represent total internal current draws when all points are ON. The current draw per point can be obtained by dividing the total value by the number of points.

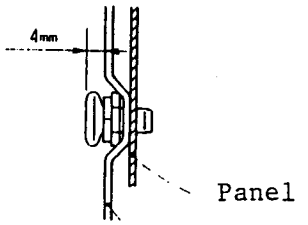


Note 1: Two input or output units can be loaded on expansion power supply unit.

Unit Installation

(1) Install CPU, expansion base and expansion power supply unit on a panel.

① When mounting expansion base units on a panel, make sure the screw head is lower than 4 mm; otherwise I/O units cannot be installed.



Applicable screw: M4 pan-head screw (spring or flat washers may be used.) (These are not attached to the unit.)

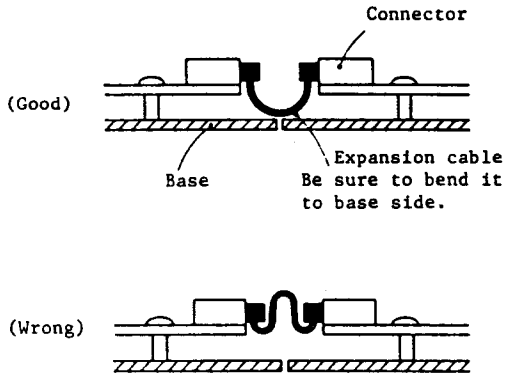
② It is recommended that a mounting plate finished with a high-conductance plating be used: this significantly improves resistance to noise.

③ When the mounting plate is finished with a coating, conductivity between the chassis of the CPU unit and expansion unit is improved if mounted to the mounting plate with screws tightened into tapped holes, thereby enhancing resistance to noise.

④ When a large current flows in the panel, insulate the mounting plate electrically from the panel and ground the mounting plate completely.

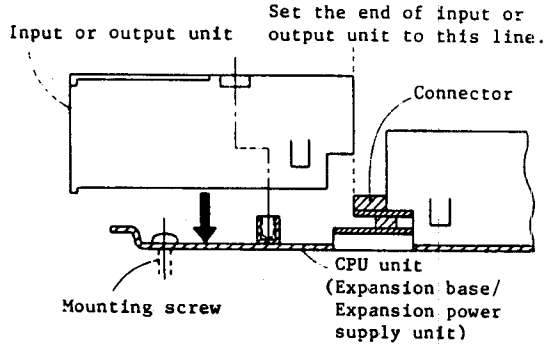
(2) Connect expansion cable.
To use an expansion base and extension power supply unit, connect bases with each other via an expansion cable (PFJ-K1, length: 30mm).

Note: Each expansion base or expansion power supply unit is provided with one expansion cable (PFJ-K1).



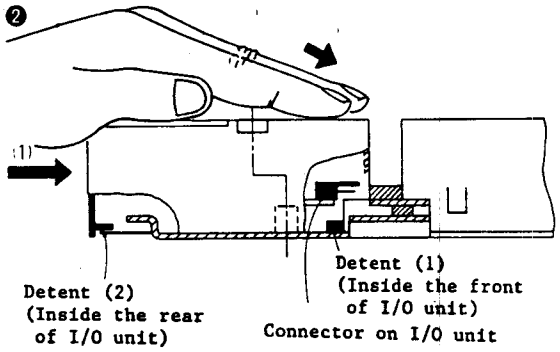
(3) Load input or output unit.

❶



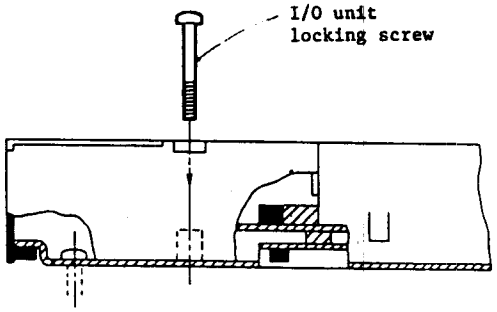
- Put input or output unit on base, setting the end of the unit to connector end on base plate.

❷



- Push the I/O unit in the direction of the arrow (1) until the unit is locked.
  Push the top of the I/O unit to plug in the connector easily.
- Detents (1) and (2) of the I/O unit slide under the bent parts of the base unit so that the I/O unit is locked.

❸

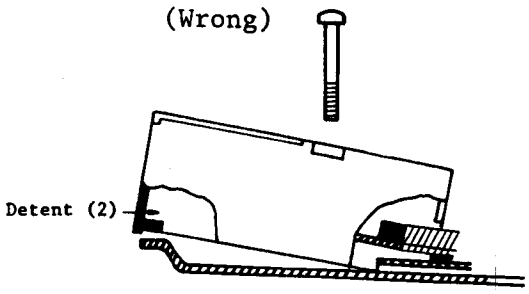


- Fasten the I/O unit to the base unit with locking screws.

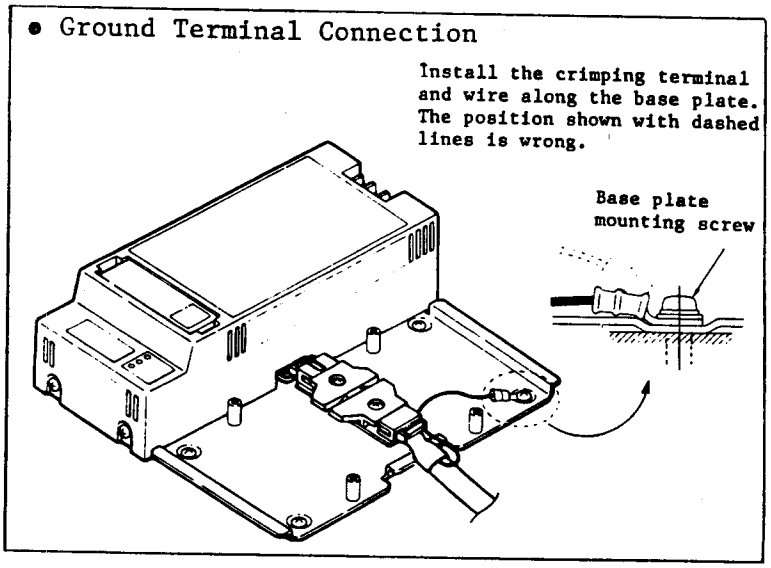
Note 1: Two screws are attached to each unit.

Note 2: Do not apply a torque exceeding 10kg to screw to avoid case deformation.

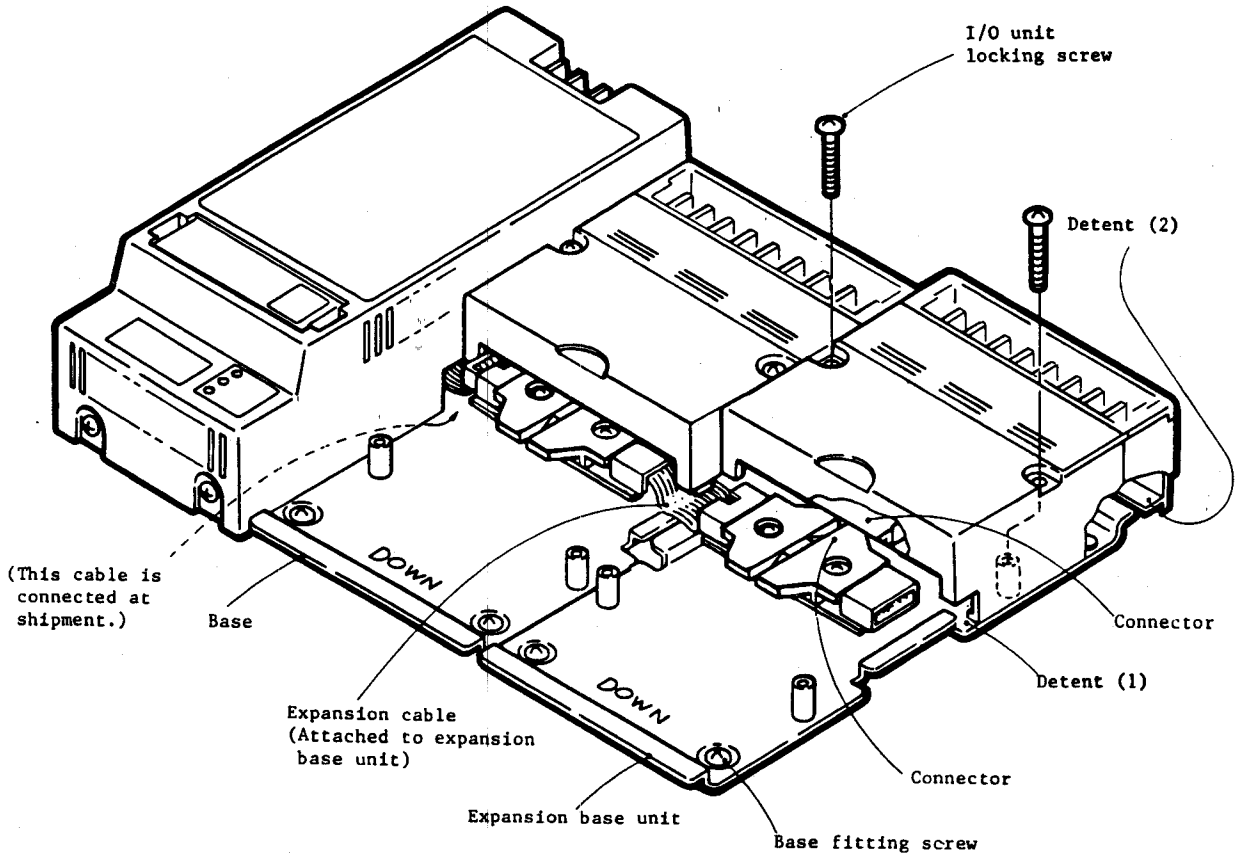
- Do not tighten the screw with detent (2) disengaged, or the connector is damaged.



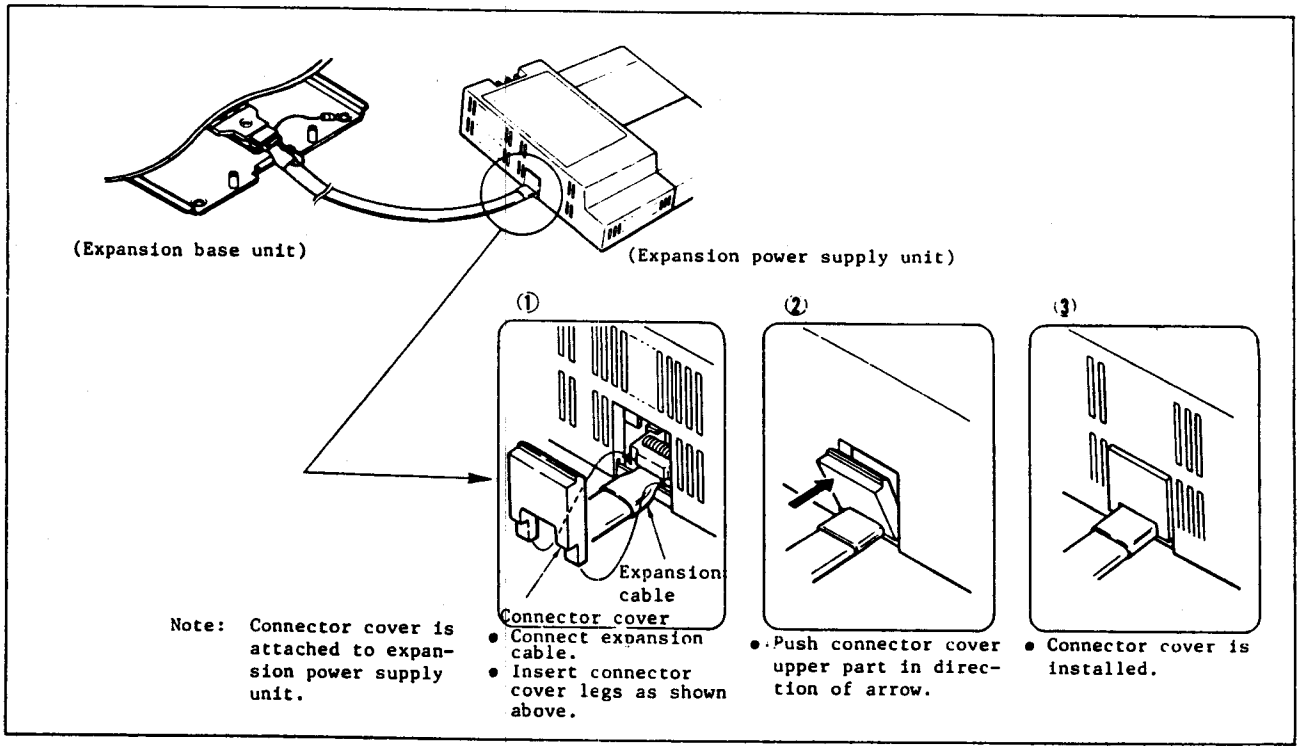
- Ground Terminal Connection



Installation Illustration



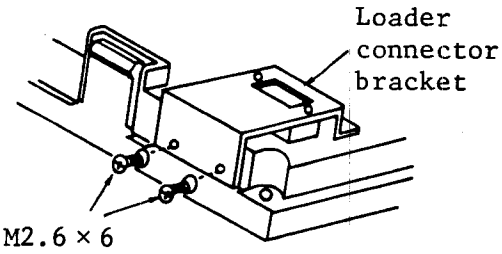
Connection of expansion cable PFA-1A21/PFA-1A22/PFA-1A23 to expansion power supply unit's expansion connector IN side



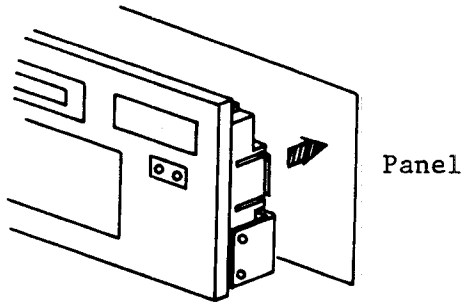
Program Loader-Panel Surface Installation

When installing the program loader to a panel surface, use the optional panel mount bracket PFA-1A41. Follow the steps below for installation.

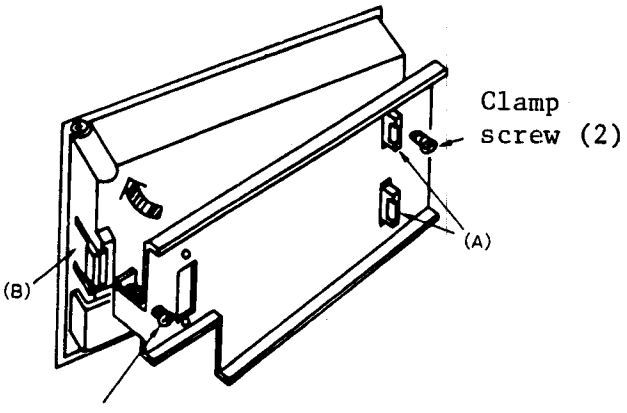
(1) Screw the loader connector bracket to the program loader.



(2) Install the loader on the panel.

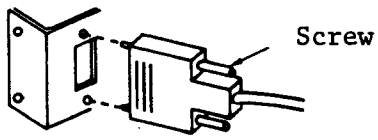


(3) Insert the protrusions on the program loader into slots (A) in the panel mount bracket, then press the panel mount bracket to the program loader until the claw (B) clicks.

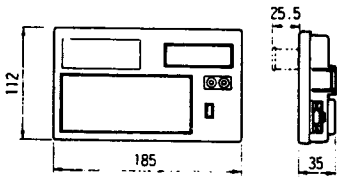


(4) Tighten the clamp screw (1) first, then (2) until the loader is secured to the panel.

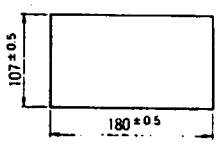
(5) Install the loader expansion cable to the connector and lock it with screws.



Dimension (mm)



Mounting hole layout



Panel thickness: 1.0-4.0

Wiring

(1) Power supply wiring

① Use a twisted pair of wires with a minimum 1.25mm^2 cross-section and make the wiring as short as possible.

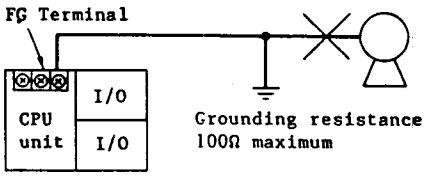
② Connect the power supply line away from the I/O signal lines and motor lines as far as possible.

If there is a possibility of electrical shocks or malfunction due to noise, take the following measures.

③ Ground the FG terminal (grounding resistance 100Ω or less).

④ Do not connect the grounding wire in common with the grounding wire for motor equipment.

⑤ Use a grounding wire with a minimum of 2mm^2 cross-section.



(2) Input wiring

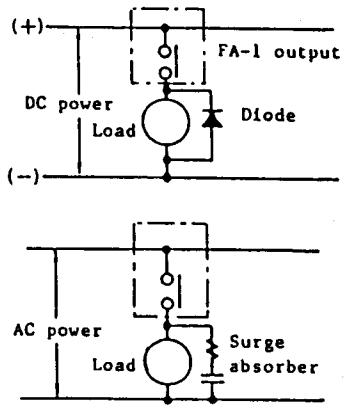
① Separate the input wiring from the output line, power supply line and motor line.

② The recommended wire size is 0.75mm^2 to 1.25mm^2. (M3.5 screw)

(3) Output wiring

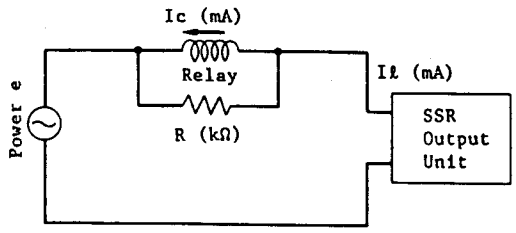
① When driving a load in which noise is generated from an electromagnet or solenoid valve, it is recommended to use a diode for DC power or a surge absorber for AC power.

② The recommended wire size is 0.75 to 1.25mm^2 (VSF or IV wire) (M3.5 screw).



③ When a small load is connected to an SSR output unit, the load may not be turned off due to the leakage current of the SSR. If this occurs, connect a resistor in parallel with the load to shunt the leakage current.

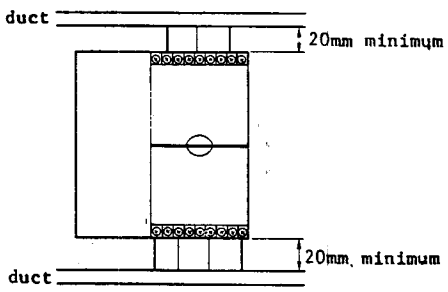
(Reference)
Formula to calculate shunt resistance



$$R \leq \frac{e}{I\ell - (Ic/4)}$$

R: Shunt resistance (kΩ)
e: Power voltage (V)
Iℓ: Max. leakage current of the SSR output unit (mA) (PFJ-T083: 6mA)
Ic: Relay coil rated current (mA)

(Duct Wiring)
When installing the I/O wiring in ducts, keep a 20mm clearance between the FA-1J and ducts for replacing I/O units.



Power Supply

(1) Power OFF

① The applicable power voltage range for the FA-1J is 85 to 264V AC or 19.2 to 28.8V DC.

② The power failure detection voltage varies with the operating conditions of the program loader and the number of I/O points used. Basically,when the power voltage drops below 85V AC or 18V DC, power failure is detected, stopping operation to prevent malfunctioning.

③ The following momentary power failures are not detected.
100V AC (50/60Hz):
1.0 cycle or less
200V AC (50/60Hz):
10 cycles or less
24V DC: 20 msec or less

(2) Inrush Current When Turning Power ON

When power to the CPU unit is turned on, the following inrush current flows.

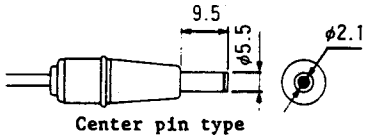
- AC Power Type: 40A maximum
(at 264V AC, maximum load)
- DC Power Type: 30A maximum
(at 28.8V DC, maximum load)

(3) AC adapter for program loader

When a program loader is independently operated, use an AC adapter with the following specifications.

- Output power supply = 9V DC 350mA or more
- Output plug
(1) Polarity

(2) Dimensions
(mm)



Center pin type

The FA-1J has various troubleshooting functions.
When the "ERROR" lamp of the CPU unit lights up, the following causes are presumed.

Cause	Remedy
① Applied supply voltage is low.	• When the supply voltage is lower than the specified value, the "ERROR" lamp lights, and the unit stops operation: always apply normal voltage.
② No memory pack is mounted in the CPU unit.	• Install a memory pack into the CPU unit correctly. When using an EPROM or E^2PROM, use a program loader to enter a correct program, then install it into the CPU unit.
③ After power is ON, the "ERROR" lamp remains lit, and no reset operation is carried out. ("ERROR" lamp OFF procedure without program loader)	• Reset the error, using the program loader, and ensure that the "ERROR" lamp goes off. [FUN] [2] [READ] [0] [ENTR] —— Lamp goes off. [FUN] [2] [READ] —— "0" is displayed. Note: When it is desired to let the "ERROR" lamp go off without using the program loader, start the CPU unit in the following manner. [FA-1J] → [RUN] → [STOP] → [RUN] Stop the FA-1J in operation once and restart it, and the "ERROR" lamp goes off. Errors other than the above remain as they are without being reset.

Cause	Remedy
④ After a correct operation has started with the "ERROR" lamp in the OFF-state, the "ERROR" lamp lights up midway.	• In this case, the following causes are presumed. 1. Hardware abnormality (Parts breakdown) 2. Excessive external noise 3. Memory pack insertion or removal with power ON **Remedy step 1** (1) Operate FUN2 to read out the error codes. Key operation FUN → 2 → READ FUN 2 PC ERR Error codes (2) Reset the error. 0 → ENTR (3) Once again, read out the error codes. FUN → 2 → READ FUN 2 PC ERR 0 In this state, error code "0" is displayed: if the FA-1J operates normally, the error is temporary, and the unit is considered to have restored its normal condition. **Remedy step 2** If an error is not cleared even when it is reset, the cause remains pending. (Refer to "Errors".) (1) If error 8 (or 9) does not disappear, it is presumed that the memory pack's (mainly the RAM pack) contents have changed: take proper steps in the following manner. Operation stop ↓ Check and correct memory pack program. ↓ Reset the error. ↓ Start operation. (2) In a system which is subject to strong noise, take corrective actions, for suppressing the noise at the source. The use of an E^2PROM or EPROM memory pack can prevent the program from being erased.

Supplementary

- Errors

Error Items		Operating Conditions	Output	Error Lamp	Error Code *1
Power failure or memory pack removal		Stop	OFF	ON when error occurs.	Lower digit 1
WDT error		Stop	OFF	——	Lower digit 2
Memory pack replacement		Stop	OFF	——	Lower digit 4
Memory diagnosis	CRC error of user's memory	Stop	OFF	ON	Lower digit 8
	CRC error of timer/counter preset value	Continue	——	——	Upper digit 1
	User memory operational code error	Stop	OFF	ON	Upper digit 2
	Keep data Sum check error	Continue	——	——	Upper digit 4
	FA-1J program error	Stop	OFF	ON	Upper digit 8

* The program loader displays the sum of error codes. The lower digit is displayed in a hexadecimal notation from 0 to F.
For error data code details, refer to Chapter 3 FUN2 on page 121.

Error item outline:

- Power failure or memory pack removal

  When supply voltage is lower than the predetermined voltage or the memory pack is not mounted in the CPU unit, the detecting operation is carried out.

- WDT error

  The time required for one scan during operation is always monitored.

- Memory pack replacement

  The detecting operation is carried out when a memory pack is replaced with one having a different program.

- Memory diagnosis

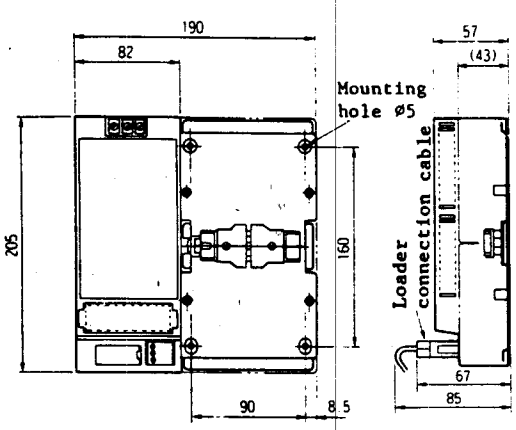
  The CPU performs self-diagnostic operation strictly on all memories used by CRC (Cyclic Redundancy Check) and sum check methods.

DIMENSION & MOUNTING HOLE LAYOUT

Dimensions

All dimensions in mm.

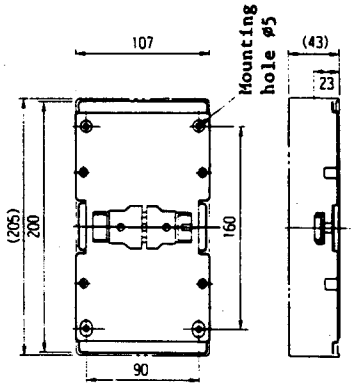
●CPU Unit/Expansion Power Supply Unit



– – – : With I/O units mounted

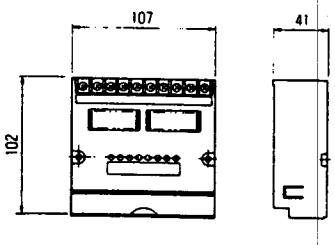
( ) : With I/O units mounting dimensions

● Expansion Base Unit

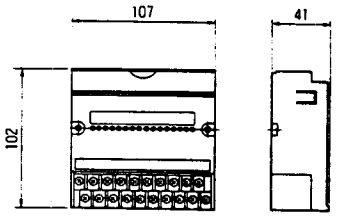


●8-I/O Unit

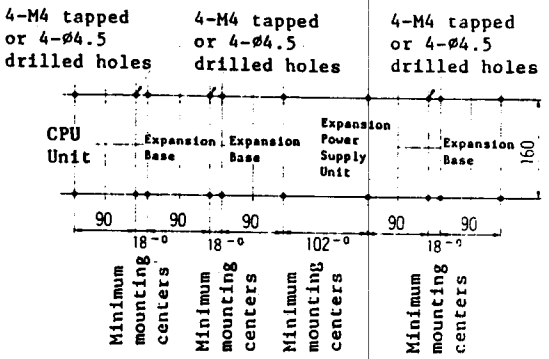
(Relay output unit differs in terminal style.)



● 16-I/O Unit

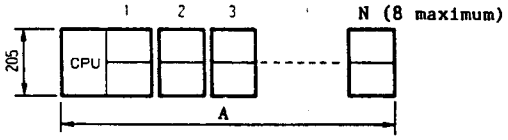


Mounting Hole Layout



(One-Row Mounting)

When mounting FA-1J units in a row, the following width is required.



● Widths

No. of Bases (N)	1	2	3	4	5	6	7	8
Dimension (A mm)	190	299	408	517	626	735	844	953

When an Expansion Power Supply Unit is included, add 83 mm to Dimension A.

Note: For dimensions and mounting hole layout of the Program Loader, see page 41.

TYPE LIST

Name			Type No.
CPU Unit	AC type		PFJ-CR1E
	DC type		PFJ-CR1DCE
Expansion Power Supply Unit	AC type		PFJ-PS1
	DC type		PFJ-PS1DC
Expansion Base Unit			PFJ-EB1
Input Unit	DC 16-input	Source type	PFJ-N161
		Sink type	PFJ-N162
	DC 8-input	Source type	PFJ-N081
		Sink type	PFJ-N082
	AC 8-input	100V AC	PFJ-N083
		200V AC	PFJ-N084
	Analog input (1 analog input)	Voltage type	PFJ-N012
		Current type	PFJ-N013
Output Unit	Relay 8-output		PFJ-T081
	Transistor output	8-output	PFJ-T082
		16-output	PFJ-T162
	SSR 8-output		PFJ-T083
	Analog output (1 analog output)	Voltage type	PFJ-T012
		Current type	PFJ-T013
Dummy Unit			PFJ-DM
Program Loader	1K steps		PFA-1H401RE
	4K steps		PFA-1H404RE
Memory Pack	E^2PROM	4K steps	PFA-1M14
	CMOS-RAM	1K steps	PFA-1M21
		4K steps	PFA-1M24
	EPROM	4K steps	PFA-1M34
Loader Extension Cable			PFA-1A11
I/O Expansion Cable	500mm long		PFA-1A21
	750mm long		PFA-1A22
	1m long		PFA-1A23
	30mm long		PFJ-K1
	90mm long		PFJ-K2
	200mm long		PFJ-K3
Double Plate	For CPU		PFJ-DP1
	For Expansion		PFJ-DP2
Panel Mount Bracket			PFA-1A41
Cassette Cable			PL-C1
Relay Removal Tool			PFA-1F11
Memory Pack Removal Tool			PFA-1F21
Output Relay			RS1S-5A
Relay Output Terminal Jumper			SSJ-4F
Transistor Output Module			RBSS-FA1
SSR Output Module			RASS-FA1
Computer Link Interface Unit			PFA-1U51

Note: IDEC's PSR series switching power supplies can be used for DC input units. For details about switching power supplies, a separate catalog is available upon request.

Chapter 2 — BASIC INSTRUCTION WORD

Instruction Word List

- Basic Instructions

Symbol	Name	Function
LOD	Load	Reads out the I/O status after storing an intermediate result.
AND	AND	Logical AND
O R	OR	Logical OR
OUT	Output	Output
MCS	Master Control Set	Starts a master control.
MCR	Master Control Reset	Ends a master control.
SOT	Single Output	Leading-edge differentiation
TIM	Timer	Timer
CNT	Counter	Counter
SFR	Shift Register	Shift register
END	End	Ends a program.
SET	Set	Sets an output, internal relay or shift register.
RST	Reset	Resets an output, internal relay or shift register.
JMP	Jump	Jumps a designated program area.
JEND	Jump End	Ends a jump program.
NOT	NOT	Inversion
FUN	Function	Sets function and computing instructions.

- FUN (Function) Instructions

FUN No.	Contents of Instructions
FUN100 to FUN146	Coincidence comparison instructions for the counter's counted values
FUN200 to FUN246	Larger/smaller comparison instructions for the counter's counted values
FUN147	Computing instruction
FUN247	Computing instruction
FUN300	Addressed jump instruction

- Computing Instructions

FUN147 (a) (a)	Type
1	BCD→BIN conversion
2	BIN→BCD conversion
3	4-digit comparison
4	Addition (+)
5	Subtraction (-)
6	Multiplication (×)
7	Division (÷)
8	Data register data shift
9	BCD digit left shift
10	Data load (16-bit)
11	Data load (8-bit)
12	Data load (indirect)
13	Data load (16-bit)
14	Data load (8-bit)
18	Data increment
19	Data decrement
20	Data store (16-bit)
21	Data store (8-bit)
22	Data store (indirect)
23	Data store (16-bit)
24	Data store (8-bit)
25	Data display (dynamic)

Instruction Format

Instructions come in two types: one-address instructions and two-address instructions.

Address	Instruction	First Address	Second Address
One-address Instructions	LOD AND OR OUT SET RST SOT	Instruction word and number	
	AND·LOD OR·LOD MCS MCR JMP JEND END	Instruction word	
Two-address Instructions	SFR SFR NOT	Instruction word and initial number	No. of bits for shift register
	TIM CNT FUN100-146 FUN200-246	Instruction word and timer/counter numbers	Preset value or comparison data
	TIM FUN CNT·FUN	Instruction word and timer/counter numbers	Output initial No.
	FUN147	Instruction word	Operation instruction code
	FUN300	Instruction word	Address No. for jump destination

FA-1J Series Allocation Numbers

Allocation of I/O, timers, counters, shift register, data register and relays are as follows:

• FA-1J Series Allocation Numbers

Name	Allocation No.	No. of Points
Input	0-7, 10-17, 20-27, 30-37, 40-47, 50-57, 60-67, 70-77, 80-87, 90-97, 100-107, 110-117, 120-127, 130-137, 140-147, 150-157	128
Output	200-207, 210-217, 220-227, 230-237, 240-247, 250-257, 260-267, 270-277, 280-287, 290-297, 300-307, 310-317, 320-327, 330-337, 340-347, 350-357	128
Internal Relay	400-407, 410-417, 420-427, 430-437, 440-447, 450-457, 460-467, 470-477, 480-487, 490-497, 500-507, 510-517, 520-527, 530-537, 540-547, 550-557, 560-567, 570-577, 580-587, 590-597, 600-607, 610-617, 620-627, 630-637, 640-647, 650-657, 660-667, 670-677, 680-687, 690-697	240
Special Internal Relay	700-707, 710-717	16
Timer	0-79 (When using arithmetic operand: 1000-1079)	80
Counter	0-44 (When using arithmetic operand: 900-944)	45
Reversible Counter	45 (dual pulse), 46 (up/down selection) (When using arithmetic operand: 945 & 946)	1 each
Shift Register	0-127 (bidirectional) (When using arithmetic operand: 1300-1427)	128
Single Output	0-95	96
Data Register	800-899 (DR0-99)	100

• FA-1J Series I/O Number Allocation

For I/O, the inputs are fixed from 0 to 157 and the outputs are fixed from 200 to 357. The I/O numbers of each expansion unit are allocated automatically in sequence beginning from those nearest to the CPU unit.

(Ex. 1) 72 I/Os

CPU	0-7 10-17 16-input	20-27 30-37 16-input	40-47 8-input
	Relay output 200-207	16-Tr. output 210-217 220-227	8-Tr. output 230-237

(Ex. 2) 40 I/Os

CPU	0- 7 10-17 16-input	Dummy	Dummy
	Relay output 200-207	Relay output 210-217	Relay output 220-227

(Ex. 3) 40 I/Os

CPU	0- 7 10-17 16-input	210-217 Relay output
	Relay output 200-207	Relay output 220-227

(Ex. 4) 32 I/Os

CPU	0-7 AC 8-input	10-17 AC 8-input	20-27 AC 8-input
	Relay output 200-207	Dummy	Dummy

(Ex. 5) 32 I/Os

CPU	0-7 AC 8-input	20-27 AC 8-input
	AC 8-input 10-17	Relay output 200-207

- **FA-1J Series Allocation Numbers of Special Relays**

No.	Function	Remarks
700	Unused	
701	Start control	
702	Start control	
703	All outputs OFF	
704	Initialize pulse (Turns ON for 1 scan when starting)	
705	Unused	
706	Numerical value error	
707	(CY) Carry & Borrow	
710	Greater than (>) comparison operation	
711	Equal to (=) comparison operation	
712	Smaller than (<) comparison operation	
713	1-sec timer reset	
714	1-sec clock (duty 1:1)	For readout only
715	100-msec clock (duty 1:1)	"
716	Timer/counter preset value changed	"
717	In-operation output	"

Supplementary

701 & 702 Start control

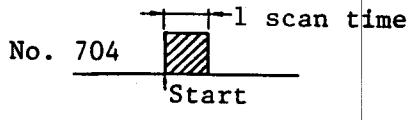
When start input of Input No. 0 is turned ON, or when automatic start is designated by setting 500 via FUN61, the FA-1J starts upon turning on special internal relay 701, and then 702. It stops when these relays are turned OFF.

703 All outputs OFF

When No. 703 is turned ON, all outputs (Nos. 200 to 357) go OFF.
The self-holding circuits using outputs (Nos. 200 to 357) also go OFF, and do not reset even when No. 703 is turned OFF. Internal relays and shift registers remain unchanged.

704 Initialize pulse

When the FA-1J starts operation, No. 704 goes ON only for one scan.



706 Numerical value error

No. 706 is turned ON when operation by a computing instruction results in a data error.

707 (CY) Carry & Borrow

Sets carry and borrow of operation result via computing instruction.

710, 711 & 712 Comparison operation

Compares designated data with those of data register via computing instruction.
No. 710 turns on when:
Register data > Operand data
No. 711 turns on when:
Register data = Operand data
No. 712 turns on when:
Register data < Operand data

713 1-sec clock reset

While No. 713 is ON, No. 714 (1-sec clock) is always placed in the reset mode.

714 1-sec clock

While No. 713 is OFF, No. 714 generates clock pulses oscillating at 500msec ON and 500msec OFF (duty ratio 1:1).

715 100-msec clock

No. 715 always generates clock pulses oscillating at 50msec ON and 50msec OFF.

716 Timer/counter preset value modified

When the program loader is used to modify timer/counter preset values for the FA-1J CPU unit, No. 716 goes ON. No. 716 is cleared when a program is written into the memory pack by pressing TRS, ENTR and ENTR keys or the memory pack is replaced.

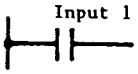
717 In-operation output

No. 717 is always ON during FA-1J operation.

LOD (Load)

Basic

- Sample relay circuit



- Program list

Address	Inst'n Word	Data
0	LOD	1
1		

- Key operation

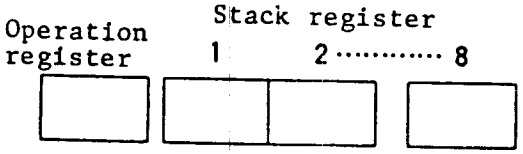
Address
0 ····· LOD 1 ENTR

- This instruction is used at the beginning of the logic.
- When a rung starts from the bus, be sure to use the LOD instruction.

Supplementary

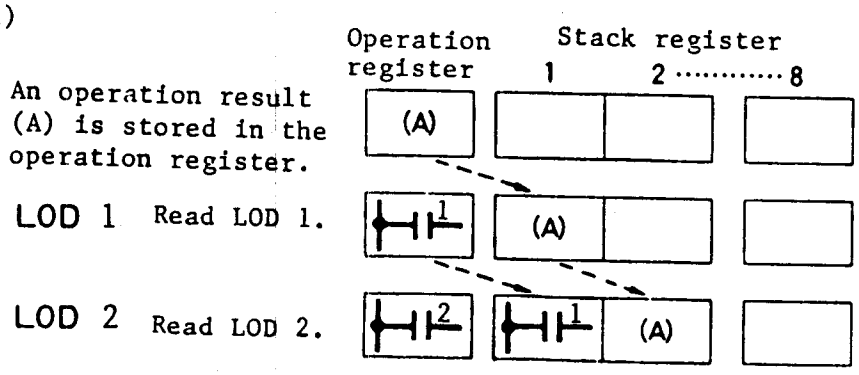
1. Operation register and stack register

The LOD instruction temporarily stores the operation result immediately before this instruction in a specific location, i.e. stack register, and then reads the input status specified by this instruction into the operation register.



The stack register is so designed that the execution of one LOD instruction shifts down the stored results by one stack register, and the execution of one AND LOD or OR LOD instruction as explained later shifts them up by one stack register. The operation results can be stored in this stack register eight times continuously.

(Example)



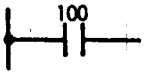
2. The following can be designated as inputs by a LOD instruction.

Function	Allocation No.
Input	0 to 157
Output status	200 to 357
Internal relay	400 to 697
Special relay	700 to 717
Timer status	0 to 79
Counter status	0 to 46
Shift register bit status	0 to 127

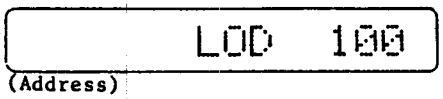
(Example)

(1) For input, output, internal and special relays

- Sample relay circuit

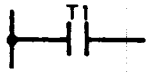


- Key operation: LOD 1 0 0 ENTR
- Loader display

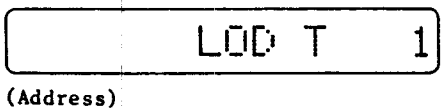


(2) For timer status

- Sample relay circuit

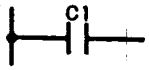


- Key operation: LOD TIM (T) 1 ENTR
- Loader display

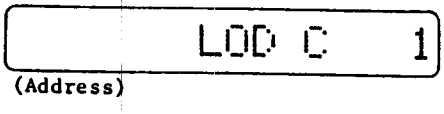


(3) For counter status

- Sample relay circuit

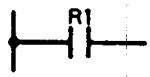


- Key operation: LOD CNT (C) 1 ENTR
- Loader display



(4) For bit status of the shift register

- Sample relay circuit

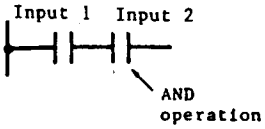


- Key operation: LOD SFR (R) 1 ENTR
- Loader display

AND (And)

Basic

● Sample relay circuit



● Program list

Address	Inst'n Word	Data
0	LOD	1
1	AND	2

● Key operation

Address
0 ····· LOD 1 ENTR
1 ····· AND 2 ENTR

● The AND instruction is a logical product instruction used for programming a series contact circuit.

Supplementary

1. AND truth table

Input 1	Input 2	Operation Result
OFF	OFF	OFF
ON	OFF	OFF
OFF	ON	OFF
ON	ON	ON

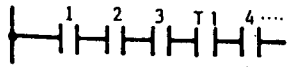
2. The following can be designated as inputs by an AND instruction.

Function	Allocation No.
Input	0 to 157
Output status	200 to 357
Internal relay	400 to 697
Special relay	700 to 717
Timer status	0 to 79
Counter status	0 to 46
Shift register bit status	0 to 127

3. Program when AND inputs continue

AND instructions can be used continuously many times.

- Sample relay circuit



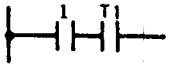
- Program list

Address	Inst'n Word	Data
0	LOD	1
1	AND	2
2	AND	3
3	AND T	1
4	AND	4

(Example)

(1) For AND input of timer status

- Sample relay circuit

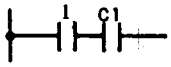


- Key operation

(Address)
0 ····· LOD 1 ENTR
1 ····· AND TIM (T) 1 ENTR

(2) For AND input of counter status

- Sample relay circuit

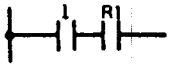


- Key operation

(Address)
0 ····· LOD 1 ENTR
1 ····· AND CNT (C) 1 ENTR

(3) For AND input of the shift register bit status

- Sample relay circuit



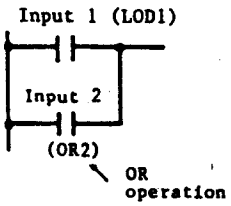
- Key operation

(Address)
0 ····· LOD 1 ENTR
1 ····· AND SFR (R) 1 ENTR

OR (Or)

Basic

- Sample relay circuit



- Program list

Address	Inst'n Word	Data
0	LOD	1
1	OR	2

- Key operation

Address
0 ····· LOD 1 ENTR
1 ····· OR 2 ENTR

- The OR instruction is a logical sum instruction used for programming a parallel contact circuit.

Supplementary

1. OR truth table

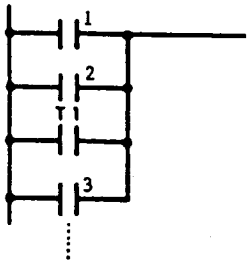
Input 1	Input 2	Operation Result
OFF	OFF	OFF
ON	OFF	ON
OFF	ON	ON
ON	ON	ON

2. The following can be designated as inputs by an OR instruction.

Function	Allocation No.
Input	0 to 157
Output status	200 to 357
Internal relay	400 to 697
Special relay	700 to 717
Timer status	0 to 79
Counter status	0 to 46
Shift register bit status	0 to 127

3. Program when OR inputs continue

OR instructions can be used continuously many times.



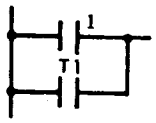
- Program list

Address	Inst'n Word	Data
0	LOD	1
1	OR	2
2	OR T	1
3	OR	3

(Example)

(1) For OR input of timer status

- Sample relay circuit

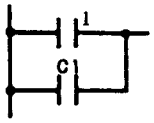


- Key operation

(Address)
0 ····· LOD 1 ENTR
1 ····· OR TIM (T) 1 ENTR

(2) For OR input of counter status

- Sample relay circuit

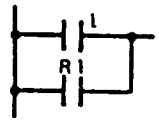


- Key operation

(Address)
0 ····· LOD 1 ENTR
1 ····· OR CNT (C) 1 ENTR

(3) For OR input of shift register bit status

- Sample relay circuit



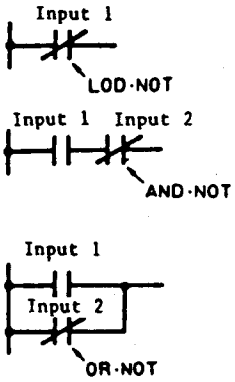
- Key operation

(Address)
0 ····· LOD 1 ENTR
1 ····· OR SFR (R) 1 ENTR

NOT (Not)

Basic

● Sample relay circuit



● Program list

Address	Inst'n Word	Data
0	LOD NOT	1

Address	Inst'n Word	Data
0	LOD	1
1	AND NOT	2

Address	Inst'n Word	Data
0	LOD	1
1	OR NOT	2

● Key operation

Address
0 ····· LOD NOT 1 ENTR

Address
0 ····· LOD 1 ENTR
1 ····· AND NOT 2 ENTR

Address
0 ····· LOD 1 ENTR
1 ····· OR NOT 2 ENTR

● The NOT instruction negates (inverts) the read input status.

This instruction is used as an auxiliary instruction for a LOD, AND or OR instruction.

Supplementary

1. NOT truth table

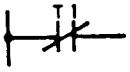
Input	Output
OFF	ON
ON	OFF

2. Fetching the input signal

When an external contact signal is connected to the input module, an NC contact in the diagram can be externally wired as an NO connection by using the NOT instruction in the program, thereby the sequence circuit can be the same as the NC contact connection.

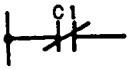
(Example)

(1) NOT input of timer status

● Sample relay circuit 

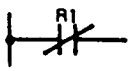
● Key operation LOD NOT TIM (T) 1 ENTR

(2) NOT input of counter status

● Sample relay circuit 

● Key operation LOD NOT CNT (C) 1 ENTR

(3) NOT input of shift register bit status

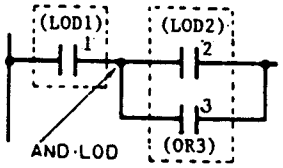
● Sample relay circuit 

● Key operation LOD NOT SFR (R) 1 ENTR

AND LOD (AND Load)

Basic

- Sample relay circuit



- Program list

Address	Inst'n Word	Data
0	LOD	1
1	LOD	2
2	OR	3
3	AND LOD	

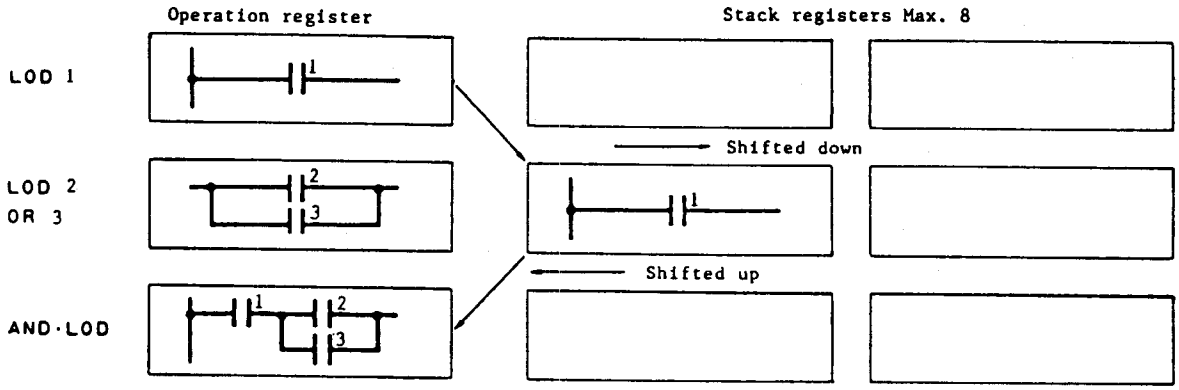
- Key operation

Address
0 ..... LOD 1 ENTR
1 ..... LOD 2 ENTR
2 ..... OR 3 ENTR
3 ..... AND LOD ENTR

- The AND LOD instruction is used to connect circuits starting with a LOD instruction in series.

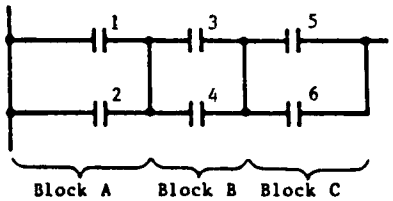
Supplementary

- Operation register and stack register status



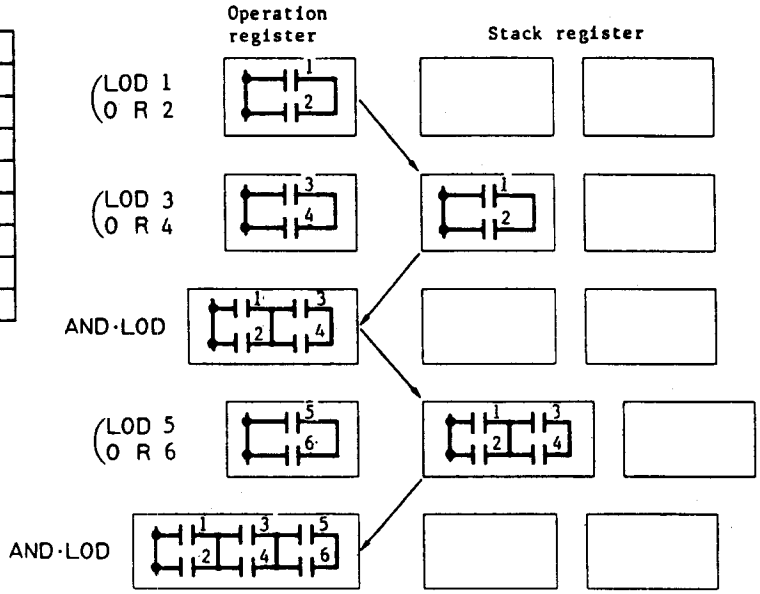
The AND LOD instruction fetches programs stored in the stack register by the LOD instruction and then ANDs them.

- For the following circuit example, the AND LOD instruction can be used in two ways.



Program 1

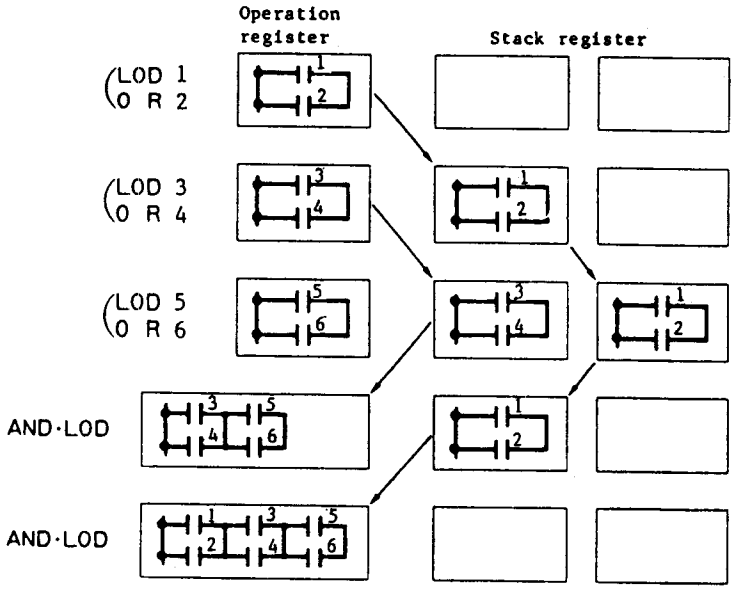
Inst'n Word	Data
LOD	1
OR	2
LOD	3
OR	4
AND LOD	
LOD	5
OR	6
AND LOD	



- Programs (Blocks A and B) stored respectively by LOD 1 and LOD 3 are fetched by the AND LOD instruction, thus forming a circuit connected in series. Then, Block C starting with LOD 5 is programmed, and the Block A/B circuits are connected in series with the Block C circuit by the AND LOD instruction.

Program 2

Inst'n Word	Data
LOD	1
OR	2
LOD	3
OR	4
LOD	5
OR	6
AND LOD	
AND LOD	



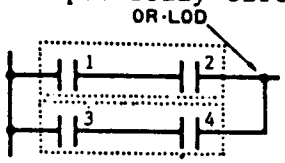
- After Blocks A, B, and C are stored in sequence, the AND LOD Instructions are used continuously two times, and the circuits of Blocks A, B, and C are connected in series sequentially.
  In this case, note the sequence of the stored circuits and the number of fetching operations. The relation between the LOD instructions used and the number of AND LOD instructions is as follows.

  Number of AND LOD instructions = Number of LOD instructions - 1

OR LOD (OR Load)

Basic

- Sample relay circuit



- Program list

Address	Inst'n Word	Data
0	LOD	1
1	AND	2
2	LOD	3
3	AND	4
4	OR LOD	

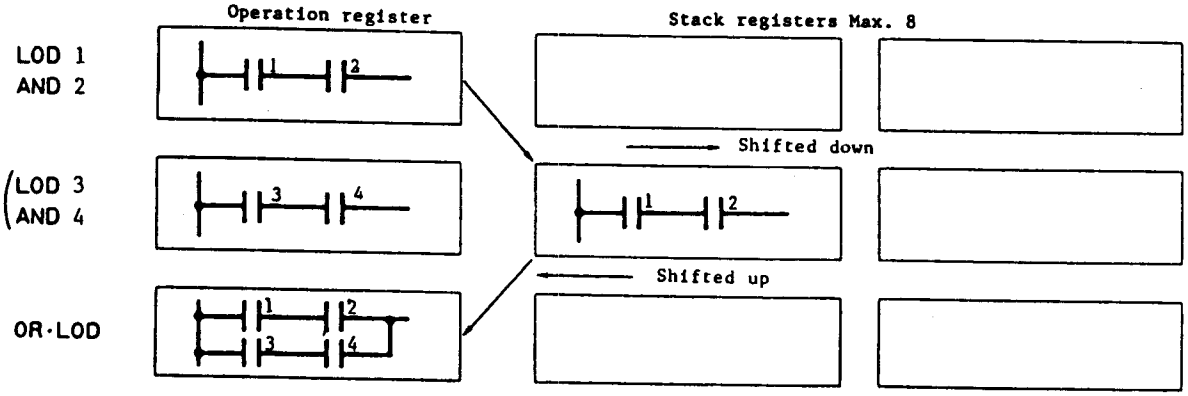
- Key operation

Address
0 ····· LOD 1 ENTR
1 ····· AND 2 ENTR
2 ····· LOD 3 ENTR
3 ····· AND 4 ENTR
4 ····· OR LOD ENTR

- The OR LOD instruction is used to connect circuits starting with LOD instructions in parallel.

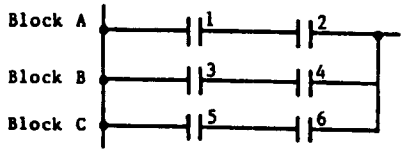
Supplementary

- Operation register and stack register status



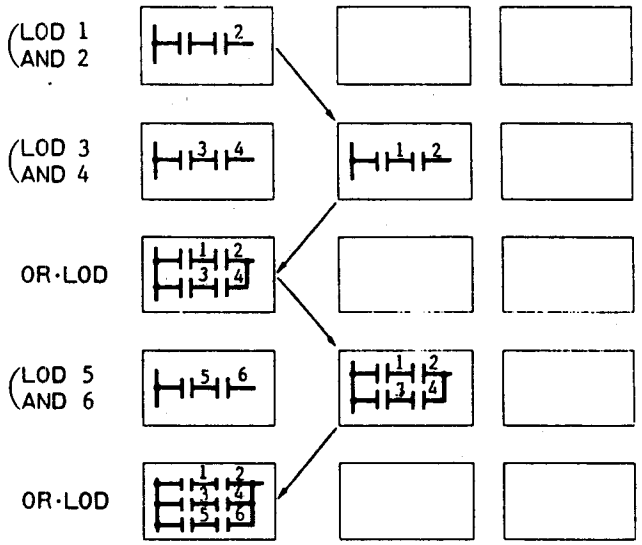
The OR LOD instruction fetches programs stored in the stack register by the LOD instruction and then ORs them.

- For the following circuit example, the OR LOD instruction can be used in two ways.



Program 1

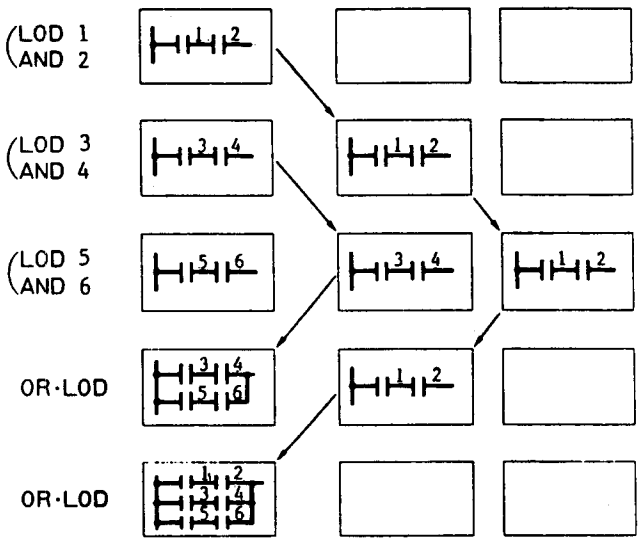
Inst'n Word	Data
LOD	1
AND	2
LOD	3
AND	4
OR LOD	
LOD	5
AND	6
OR LOD	



- Programs (Blocks A and B) stored respectively by LOD 1 and LOD 3 are fetched by the OR LOD instruction, thus forming a circuit connected in parallel. Then, Block C starting with LOD 5 is programmed, and the Block A/B circuits are connected in parallel with the Block C circuit by the OR LOD instruction.

Program 2

Inst'n Word	Data
LOD	1
AND	2
LOD	3
AND	4
LOD	5
AND	6
OR LOD	
OR LOD	



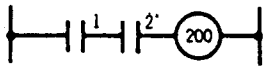
- After Blocks A, B, and C are stored in sequence, the OR LOD Instructions are used continuously two times, and the circuits of Blocks A, B, and C are connected in parallel sequentially.
  In this case, note the sequence of the stored circuits and the number of fetching operations. The relation between the LOD instructions used and the number of OR LOD instructions is as follows.

  Number of OR LOD instructions = Number of LOD instructions - 1

OUT (Output)

Basic

- Sample relay circuit
- Program list



Address	Inst'n Word	Data
0	LOD	1
1	AND	2
2	OUT	200

- Key operation

Address
0 ..... LOD 1 ENTR
1 ..... AND 2 ENTR
2 ..... OUT 2 0 0 ENTR

- The logical operation result immediately before the OUT instruction is outputted to the designated output number.

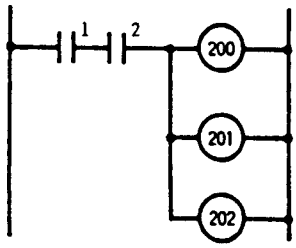
Supplementary

1. The following can be designated as outputs by the OUT instruction.

Function	Allocation No.
Output	200 to 357
Internal relay	400 to 697
Special relay	700 to 713

2. Programs with continuous OUT instructions

OUT instructions can be programmed continuously.
There is no limit to the number of OUT instructions to be programmed continuously.



Inst'n Word	Data
LOD	1
AND	2
OUT	200
OUT	201
OUT	202

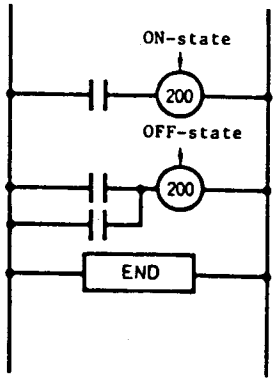
3. Double setting of OUT instruction (Double programs)

- In the FA-1J, the same output numbers (Nos. 200 to 357) can be programmed more than once.
  This is because some programs require this function, for example, when a program is shifted using the addressed Jump instruction (described later).
- When the ENTR key is pressed for the second and subsequent OUT instructions, a buzzer sounds, signalling a double program, but the writing operation is performed.
- Double setting of internal and special relays is not possible.

CAUTION

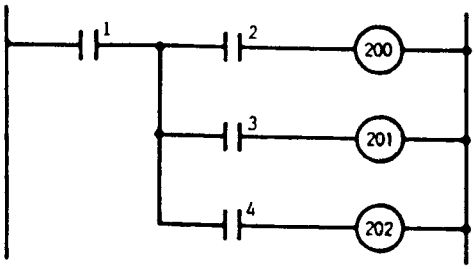
1. Precautions against output double setting

   When the same output number is programmed more than once within one scan inadvertently, the output status nearest to the END instruction is given top priority for outputting.



   In this example, output 200 is OFF. Under this condition, if output 200 is monitored, it is blinking at random.

2. The following circuit cannot be programmed.



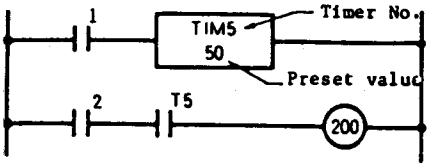
TIM (Timer)

Timer Nos. 0 to 79 are 100msec subtracting timers.

100msec timer

Basic

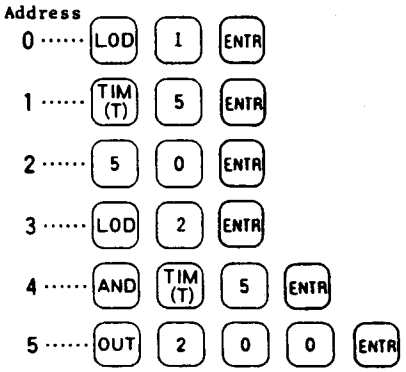
- Sample relay circuit



- Program list

Address	Inst'n Word	Data
0	LOD	1
1	TIM	5
2		50
3	LOD	2
4	AND T	5
5	OUT	200

- Key operation

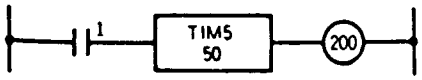


- Timer preset values are 0 to 9999.
- When timer instructions are programmed, two addresses are always required. A timer instruction and timer No. should be set at the first address, and the preset value should be set at the second address (always the next address).

Supplementary

1. • When the operation result immediately before this instruction (which is a timer input) is ON, clock pulse counting is initiated.
   • When the counted value reaches the preset time, the timer output turns ON.
   • When the timer input is OFF, the preset value is set.
   • After the time up, the counted value remains at 0 until the timer input turns OFF.
   • The timer cannot use the same number in double. (An error message is displayed when the program is inputted.)
   • If the preset value is changed during subtraction, the timer remains unchanged with the previous preset time for that cycle, and is changed from the next time cycle. (However, if the preset value is changed to 0, the timer stops operation, immediately turning the output ON.)

2. The output can be fetched immediately after the TIM instruction.



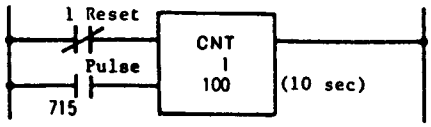
Address	Inst'n Word	Data
0	LOD	1
1	TIM	5
2		50
3	OUT	200

3. Timer accuracy

Error	Maximum	+3 scan time
	Minimum	-100 msec + 1 scan time
Fluctuations when a 1-sec timer is made (1 scan = 30 msec)		+9% to -7%

4. Power failure memory type timer

- An ordinary timer does not have power failure memory protection: a timer can be formed, using the 100-msec special internal relay (715) or the 1-sec clock (714) and a CNT instruction.



Address	Inst'n Word	Data
0	LOD N	1
1	LOD	715
2	CNT	1
3		100

Note: In this case, it is necessary to designate the counter to be held at the starting time using FUN7.

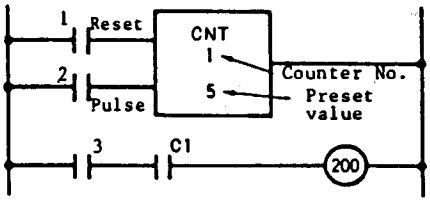
CNT (Counter)

- Two types of counters can be selected, depending on their numbers.
  ① Counter Nos. 0 to 44 are adding counters.
  ② Counter Nos. 45 and 46 are reversible counters.

1. Adding counter

Basic

- Sample relay circuit



- Program list

Address	Inst'n Word	Data
0	LOD	1
1	LOD	2
2	CNT	1
3		5
4	LOD	3
5	AND C	1
6	OUT	200

- Key operation

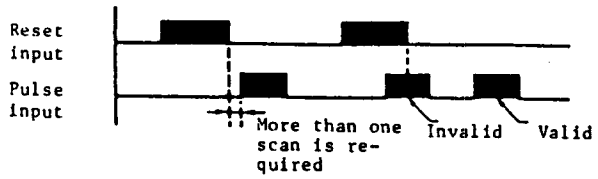
Address
0 ····· LOD 1 ENTR
1 ····· LOD 2 ENTR
2 ····· CNT (C) 1 ENTR
3 ····· 5 ENTR
4 ····· LOD 3 ENTR
5 ····· AND CNT (C) 1 ENTR
6 ····· OUT 2 0 0 ENTR

- 45 adding counters are available: Nos. 0 to 44.
- The counter should be programmed in the order of reset input, pulse input and CNT instruction.
- The counter preset values are 0 to 9999.

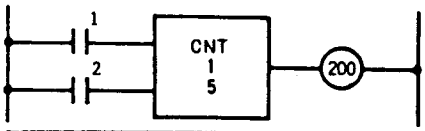
Supplementary

1. • When the counter instruction is programmed, two addresses are always required. For the first address, set the counter instruction and counter No., and for the second address, set the preset value.
   • The same number cannot be used in double.
   • While the reset input is OFF, the counter counts the leading edges of pulse inputs, and compares them with the preset value. When the counted value reaches the preset value, the counter turns output ON and the output remains ON until the reset input is turned ON.
   • When the reset input is changed from OFF to ON, the counted value is reset; while the reset input is ON, all pulse inputs are ignored.
   • When power is OFF, the counter's counted value can be held using the FUN (function) designation. (Refer to FUN7). ... (This designates whether the value should be cleared or held at the starting time.)

- Since the reset input has priority, the counter counts only the pulse input which has changed from OFF to ON subsequent to one scanning after the reset input changed from ON to OFF.



2. The output can be fetched immediately after the CNT instruction.



Address	Inst'n Word	Data
0	LOD	1
1	LOD	2
2	CNT	1
3		5
4	OUT	200

3. Counter response performance

The counter response performance depends on the scan time.

The response speed S[cps] is:

$$S = \frac{1{,}000}{(\text{Scan time [msec]} + \text{Input response time [msec]}) \times 2} \text{ [cps]}$$

- Input response time

ON delay time	7 msec
OFF delay time	11 msec

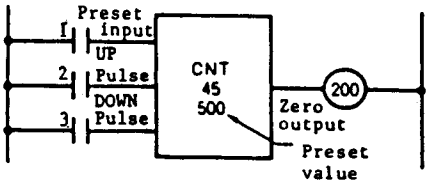
2. Reversible counter

The reversible counters have two types: one is the dual-pulse type (A) having UP and DOWN pulse inputs, and the other is the UP/DOWN selection type (B) with only one pulse input, which switches the up/down gate.

A. Dual-pulse type reversible counter (Counter No. 45)

Basic

- Sample relay circuit



- Program list

Address	Inst'n Word	Data
0	LOD	1
1	LOD	2
2	LOD	3
3	CNT	45
4		500
5	OUT	200

- Key operation

Address

0 ····· LOD 1 ENTR

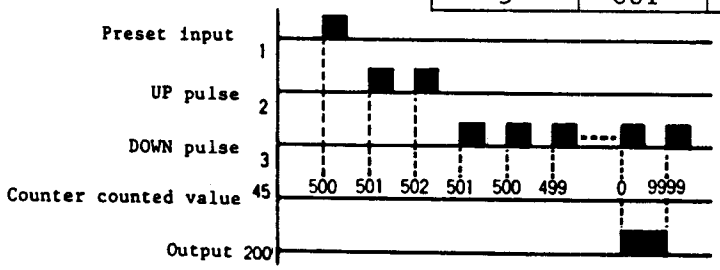
1 ····· LOD 2 ENTR

2 ····· LOD 3 ENTR

3 ····· CNT (C) 4 5 ENTR

4 ····· 5 0 0 ENTR

5 ····· OUT 2 0 0 ENTR



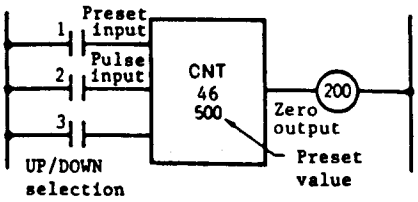
Supplementary

- When the UP pulse and DOWN pulse are ON simultaneously, it may cause the counter not to perform the counting operation.
- Three inputs, i.e. preset input, UP pulse and DOWN pulse are required.
- When the preset input is ON, the preset value is set, and when the preset input is OFF, counting is started.
- The counter output is ON only when the counted value is "0".
- After the counted value reaches 0 or 9999, it changes from 0 to 9999 or from 9999 to 0.
- When a reversible counter is initially programmed and operated, the preset value becomes unconstant (the value remains unsteady) if the preset input is not turned ON; therefore, be sure to design the circuit such that the preset input enters before the counting operation starts.

B. UP/DOWN selection type reversible counter (Counter No. 46)

Basic

● Sample relay circuit



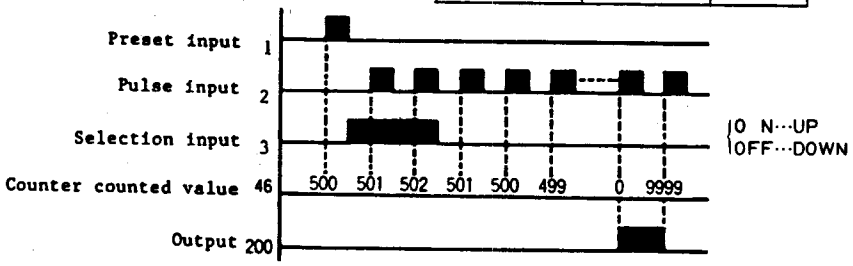
● Program list

Address	Inst'n Word	Data
0	LOD	1
1	LOD	2
2	LOD	3
3	CNT	46
4		500
5	OUT	200

● Key operation

Address

0 ····· LOD 1 ENTR
1 ····· LOD 2 ENTR
2 ····· LOD 3 ENTR
3 ····· CNT (T) 4 6 ENTR
4 ····· 5 0 0 ENTR
5 ····· OUT 2 0 0 ENTR



Supplementary

- The UP/DOWN mode is selected for UP when the UP/DOWN selection input is ON and DOWN when it is OFF.

  ON : UP count
  OFF: DOWN count

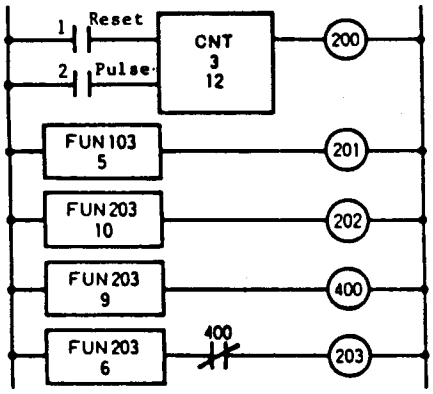
- The same counter number cannot be used in double.
- When the preset value is changed during counter operation, the new preset value becomes effective immediately. (However, the counter does not operate even if the preset value is changed after the preset value has been reached.)

FUN100 to FUN146 Coincidence comparison instruction for counted values

FUN200 to FUN246 Larger/smaller comparison instruction for counted values

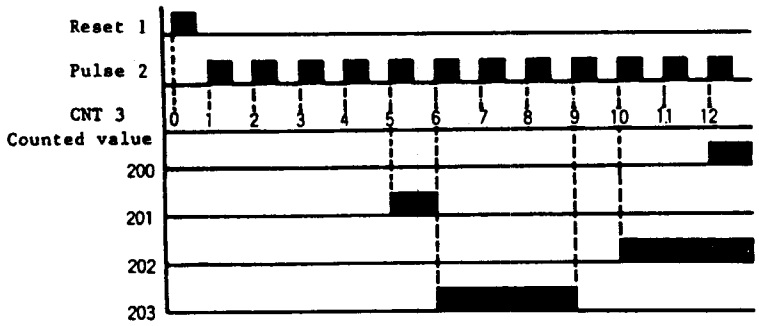
Basic

- Counter multistage setting example



- Program list

Address	Inst'n Word	Data	Address	Inst'n Word	Data
0	LOD	1	9		10
1	LOD	2	10	OUT	202
2	CNT	3	11	FUN	203
3		12	12		9
4	OUT	200	13	OUT	400
5	FUN	103	14	FUN	203
6		5	15		6
7	OUT	201	16	AND NOT	400
8	FUN	203	17	OUT	203

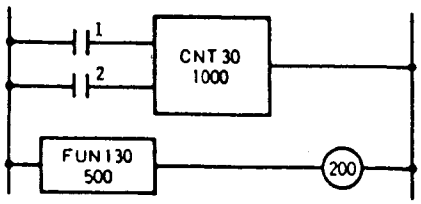


- 47 counters (0 to 46) can perform coincidence comparison and larger/smaller comparison operations with respect to optional values.
- Corresponding to counter Nos. 0 to 46, FUN100 to FUN146 (Counter No. + 100) are coincidence comparison instructions and FUN200 to FUN246 (Counter No. + 200) are larger/smaller comparison instructions.

Supplementary

1. • Regardless of the status of the counter, this instruction merely compares the counted value.
   • Both comparison instructions have the same function as the LOD instruction but they do not have a function corresponding to the AND and OR instructions; therefore, insert an internal relay, for example, whenever necessary.
   • The same FUN number can be used repeatedly for different preset values.

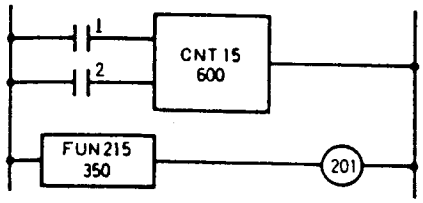
2. Sample program for coincidence comparison



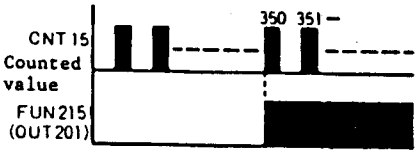
Inst'n Word	Data
LOD	1
LOD	2
CNT	30
	1000
FUN	130
	500
OUT	200

Output 200 is turned ON when Counter 30 counted value = 500.

3. Sample program 1 for larger/smaller comparison

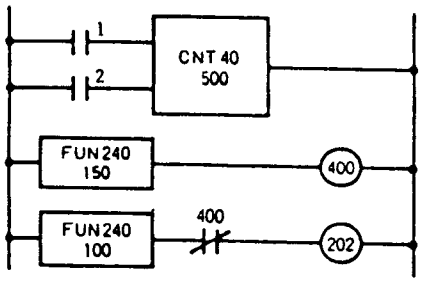


Inst'n Word	Data
LOD	1
LOD	2
CNT	15
	600
FUN	215
	350
OUT	201

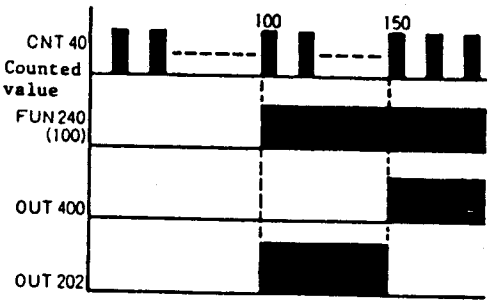


Output 201 is turned ON when Counter 15 counted value ≥ 350.

4. Sample program 2 for larger/smaller comparison



Inst'n Word	Data
LOD	1
LOD	2
CNT	40
	500
FUN	240
	150
OUT	400
FUN	240
	100
AND N	400
OUT	202

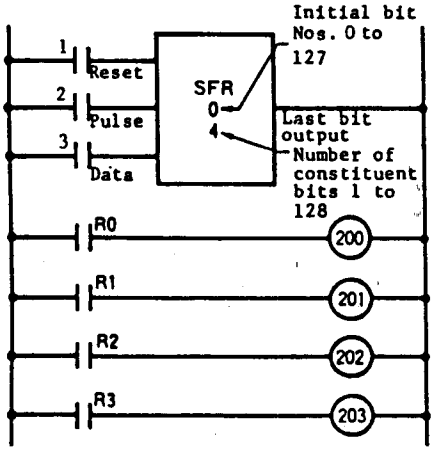


Output 202 is turned ON when Counter 40 counted value is between 100 and 150.

SFR (Shift register in forward direction)

Basic

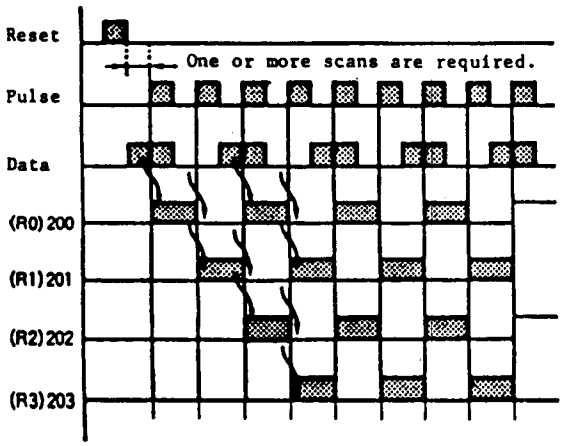
• Sample relay circuit



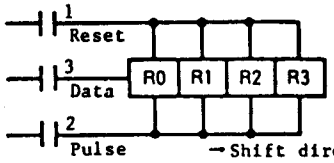
• Program list

Address	Inst'n Word	Data	
0	LOD	1	
1	LOD	2	
2	LOD	3	
3	SFR	0	← Initial bit
4		4	← 4-bit configuration
5	LOD R	0	← Deriving Bit 0 status
6	OUT	200	
7	LOD R	1	← Deriving Bit 1 status
8	OUT	201	
9	LOD R	2	← Deriving Bit 2 status
10	OUT	202	
11	LOD R	3	← Deriving Bit 3 status
12	OUT	203	

• Time chart

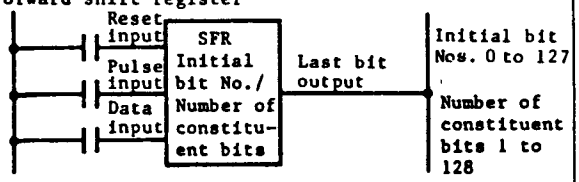


• Structural concept



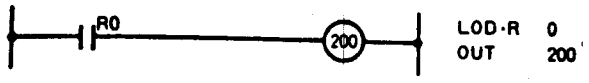
- The shift register has a total of 128 bits, and an optional number of shift register instructions can be formed.
- Shift registers should be programmed in the order of reset input, pulse input, data input, and shift register instruction.
- The shift register uses one point for one bit and requires two addresses for programming. The initial bit number of the SFR should be set at the first address and the number of constituent bits at the second address.

Forward shift register

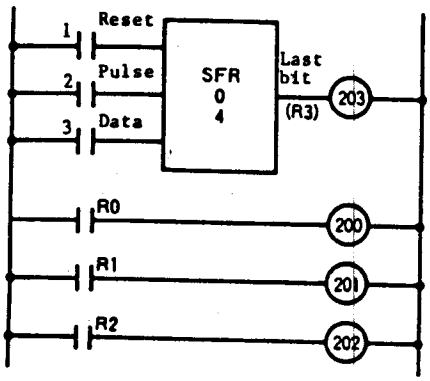


Supplementary

1. Each bit status can be outputted, using the LOD R instruction.

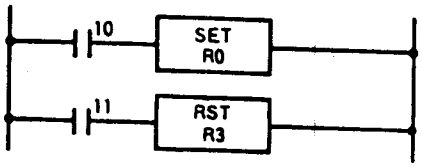


- The last bit status can be outputted subsequent to the SFR instruction.



Address	Inst'n Word	Data	
0	LOD	1	
1	LOD	2	
2	LOD	3	
3	SFR	0	
4		4	
5	OUT	203	← Deriving the last bit output
6	LOD R	0	} Deriving each bit output
7	OUT	200	
8	LOD R	1	
9	OUT	201	
10	LOD R	2	
11	OUT	202	

- An optional bit can be turned ON (SET) or OFF (RST), using the SET or RST instruction.



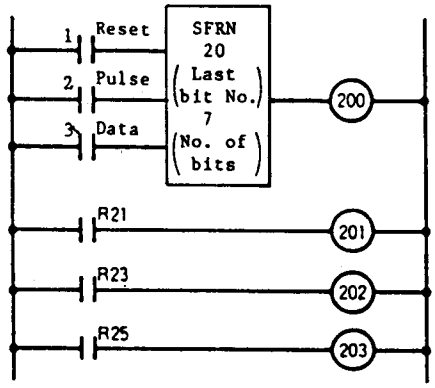
The SET or RST instruction is actuated, depending on the optional input conditions.
The optional bit No. to be turned ON or OFF should be designated with the SET or RST instruction.

SFR NOT

Shift register in reverse direction

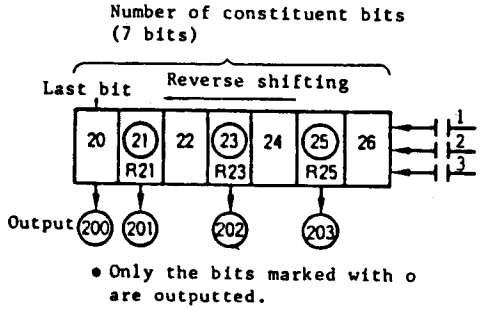
Basic

● Sample relay circuit



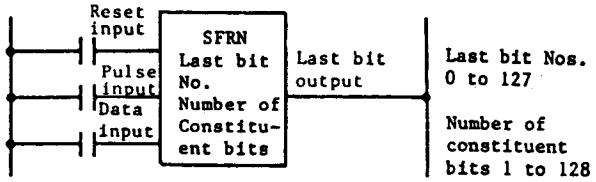
● Program list

Inst'n Word	Data	
LOD	1	
LOD	2	
LOD	3	
SFR N	20	← Last bit
	7	← 7-bit configuration
OUT	200	
LOD R	21	← Deriving Bit 21 status
OUT	201	
LOD R	23	← Deriving Bit 23 status
OUT	202	
LOD R	25	← Deriving Bit 25 status
OUT	203	



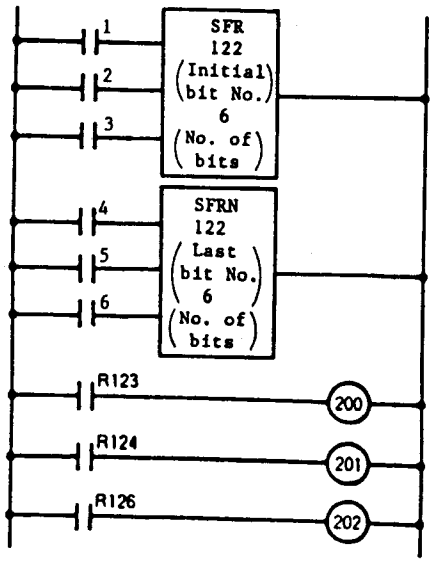
● Only the bits marked with o are outputted.

● For the reverse shifting, use the SFR NOT instruction and program the last bit No. at the first address.

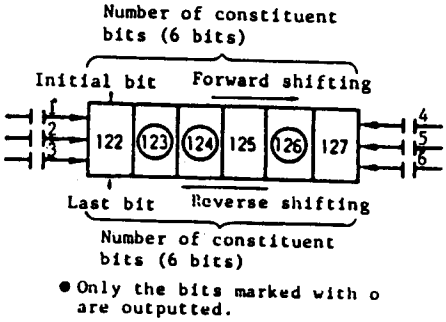


Supplementary

- A bidirectional shift register can be constituted by combining a forward shift register and a reverse shift register.
- Example of a bidirectional shift register



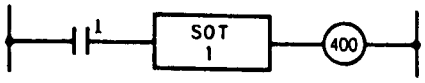
Inst'n Word	Data
LOD	1
LOD	2
LOD	3
SFR	122
	6
LOD	4
LOD	5
LOD	6
SFR N	122
	6
LOD R	123
OUT	200
LOD R	124
OUT	201
LOD R	126
OUT	202



SOT (Single output)

Basic

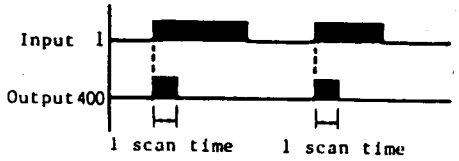
- Sample relay circuit



- Program list

Address	Inst'n Word	Data
0	LOD	1
1	SOT	1
2	OUT	400

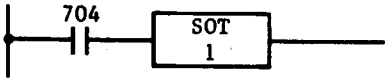
- The instruction converts (differentiates) the input signal to a one-shot signal.
- The SOT turns the SOT output ON only for a period of one scan when the input signal is turned ON.
- When a relay output is designated, it may not operate depending on the scan time.
- 96 SOT instructions (0 to 95) can be used.

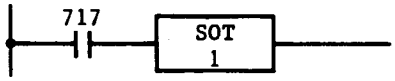


Note 1: If operation is started with input signal ON, the SOT output does not turn ON. To turn on the SOT output, input signal must turn on after starting operation.

Note 2: If an SOT instruction is used between MCS and MCR instructions and input signal to the SOT instruction turns ON before or at the same time as the input signal to the MCS instruction, the SOT output does not turn ON.

Note 3: If special relay 704 (initialize pulse) or 717 (in-operation output) is used as input signal to the SOT instruction, the SOT output does not turn ON.



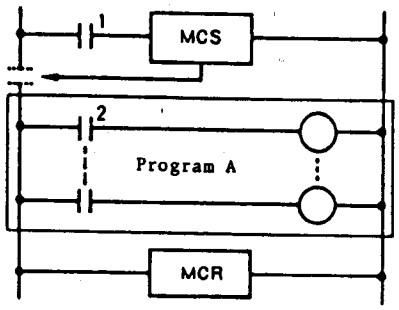


MCS (Master control set)

MCR (Master control reset)

Basic

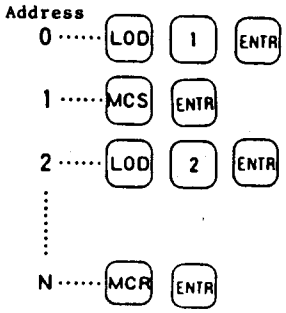
- Sample relay circuit



- Program list

Address	Inst'n Word	Data
0	LOD	1
1	MCS	
2	LOD	2
3		
N	MCR	

- Key operation



- If the input to the MCS instruction is OFF, all inputs of the program (Program A) read after the MCS instruction are forced OFF until the MCR instruction is executed: if the input to the MCS instruction is turned OFF, the program (Program A) up to the MCR is inhibited from operating.
- The MCS instruction should be used in combination with the MCR instruction.

Supplementary

1. Input conditions cannot be set for the MCR instruction.
   When the MCS ends with an MCR (or END), all values of the logical operation value stack register are turned OFF. An END instruction has the same function as the MCR instruction.

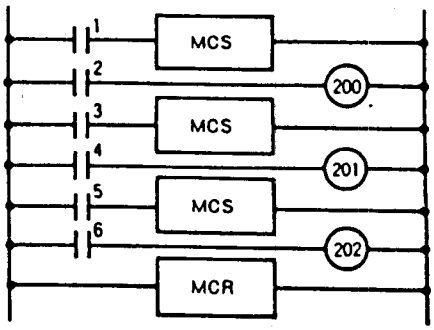
2. Status of each instruction during an MCS instruction execution

Instruction	Status
SOT, OUT	• All instructions are turned OFF.
SET, RST	• All instructions are kept.
TIM	• Counted values and outputs are reset
CNT, SFR	• Counted values are kept. • Pulse inputs are turned OFF. • Outputs are turned OFF.

Note: The MCS instruction execution means that the input conditions are in the off-state.

3. More than one MCS instruction can be set for one MCR instruction.

(Example)



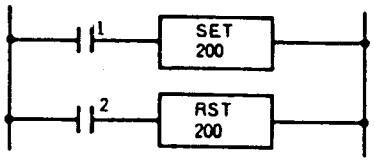
The above master control circuit gives priority to Input 1, Input 3, and Input 5 in this order.

SET (Set)

RST (Reset)

Basic

- Sample relay circuit



- Program list

Address	Inst'n Word	Data
0	LOD	1
1	SET	200
2	LOD	2
3	RST	200

- Key operation

Address

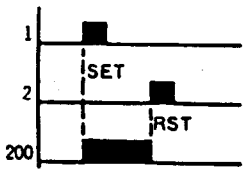
0 ····· LOD 1 ENTR

1 ····· SET 2 0 0 ENTR

2 ····· LOD 2 ENTR

3 ····· RST 2 0 0 ENTR

- Outputs, internal relays and shift registers can be set (ON) or reset (OFF), using the SET or RST instruction.



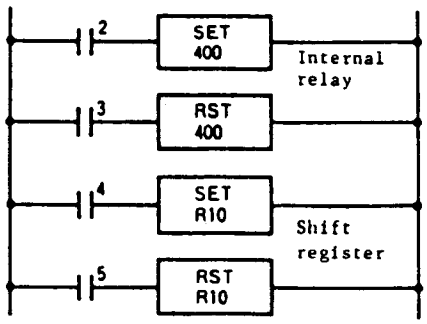
Supplementary

1. The range in which the SET RST instructions can be used.

Function	Number
Output	200 to 357
Internal relay	400 to 697
Special relay	700 to 713
Shift register	0 to 127

Note: SET and RST instructions operate only when the input signal is changed from the off-state to the on-state.

2. Sample program



Inst'n Word	Data
LOD	2
SET	400
LOD	3
RST	400
LOD	4
SET	R10
LOD	5
RST	R10

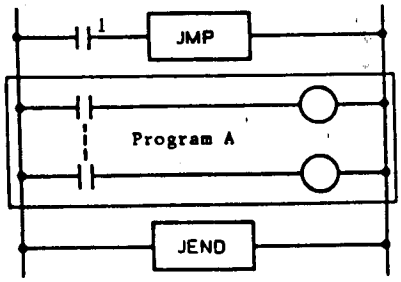
3. Double application of SET/RST instructions
The same output can be set in double for SET and RST instructions.

JMP (Jump)

JEND (Jump end)

Basic

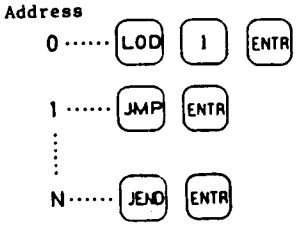
- Sample relay circuit



- Program list

Address	Inst'n Word	Data
0	LOD	1
1	JMP	
	Program A	
N	JEND	

- Key operation



- If the operation result immediately before the JMP instruction is ON, the JMP becomes valid, thus executing the program before the JEND instruction without processing (holding all statuses): if the result is OFF, the JMP becomes invalid, whereby the next program is executed.

Supplementary

1. It is impossible to program a pair of JMP and JEND instructions between another pair of JMP and JEND instructions.

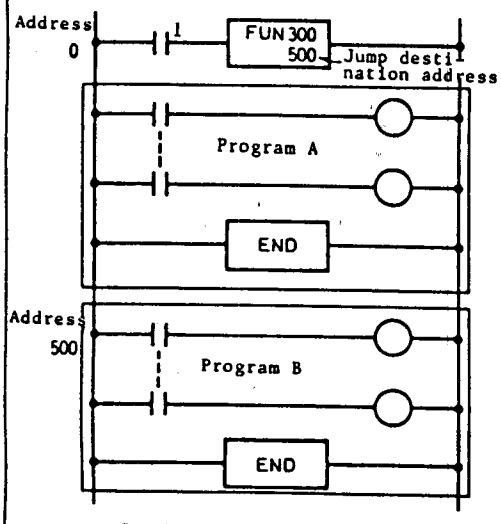
2. During a JMP instruction execution, the status between the JMP and JEND is held.
   - Outputs, internal relays, timers, counters, and shift registers, are all held in their current statuses.
   - Timer/counter counted values are also held.
   - SOT instructions are all turned OFF.

3. The difference between MCS and JMP is that the program within the JMP instruction is not executed: for example, if the output is ON beforehand, it is being maintained during the execution of the JMP instruction.

FUN300 (Addressed jump instruction)

Basic

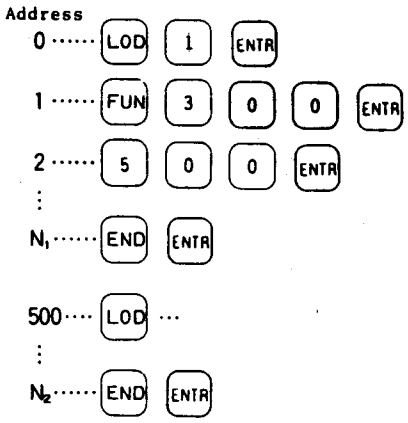
- Sample relay circuit



- Program list

Address	Inst'n Word	Data
0	LOD	1
1	FUN	300
2		500
N1	END	
500	LOD	
N2	END	

- Key operation



- If the operation result immediately before this instruction is ON, the program jumps to the designated address (jump destination address), and it is executed from the designated address. If the result is OFF, this instruction is disregarded, and the next instruction is executed.

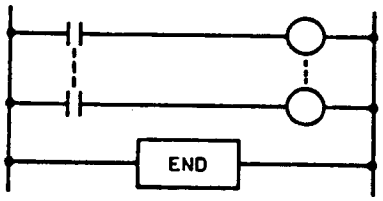
Supplementary

1. Programming is impossible if the jump destination address is not an address subsequent to the address in which this instruction is set.
2. When a program is modified, be sure to modify the jump destination address. (No automatic modification is made.)
3. The END instruction is required for each program end. Thus, one of the programs will be executed.
4. While a FUN300 instruction is executed, operating conditions before the execution are maintained at addresses between the FUN300 and jump destination.
   However, if jump has been executed during timer operation and the timer input is ON when the timer operation is restored, the counted value of the timer is indefinite.
5. If the input to SOT or CNT instruction at the jump destination is already ON or turns ON simultaneously with jump execution, the input is not turned ON or accepted. After turning OFF, the subsequent input is accepted.
6. Programs skipped by a JUMP instruction are not included in the scan time.

END (End)

Basic

- Sample relay circuit



- Program list

Address	Inst'n Word	Data
0		
1		
2		
N	END	

- This instruction is always required at the end of a program.

Supplementary

1. When the user's memories are all cleared, an END is written at all addresses.

2. • Execution of instructions from address 0 of the program memory to the address in which the END instruction is written is referred to as a scan. The time required for this execution is referred to as the scan time. Therefore, the scan time varies, depending on the address in which the END instruction is located.

   • The END instruction transfers the results processed within one scan for every END instruction to the output, and then reads in the status of the input in preparation for the next scanning operation.

External Preset Function

Preset values of timer (TIM) and counter (CNT) instructions programmed in the FA-1J and counter coincidence and greater/smaller comparison instructions can be set via digital switch installed externally.

Specifications

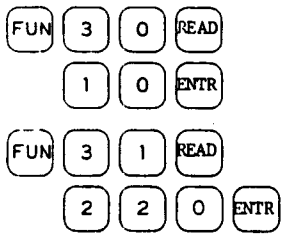
Preset type	BCD multiple setting
No. of circuits	Max. 16 (BCD 4 digits)
No. of I/Os (per circuit)	DC input unit (Source type): 4 Transistor output: 4
Applicable digital switch	Binary digital switch (with diode). Install diodes (for switching) according to the connection diagram. (Ex.) IDEC's type DF( )( )-031D(K) Diode Rating: Reverse voltage 80V min. Average rectifying current 100mA min. Lead diameter 0.5 to 0.6mm

Programming Method

- Use FUN70 to FUN85 as data of instruction words.
- Allocate initial input and output numbers via function setting FUN30 and 31.
- I/O number allocation example

  When initial input number for FUN30 is 10 and initial output number for FUN31 is 220

- Key operation



Note: 4n I/Os are allocated continuously for external presetting starting from the initial I/O No. according to designation by FUN70 to 85. FUN numbers cannot be designated intermittently, such as FUN70 followed by FUN73.

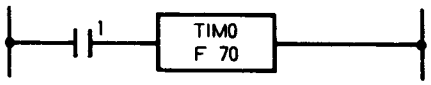
- I/O allocation for the above setting

FUN No. Corresponding to Digital Switch	Input No.	Output No.
FUN70	10-13	220-223
FUN71	14-17	224-227
FUN72	20-23	230-233
⋮	⋮	⋮
FUN85	⋮	⋮
Digital switch	A-D	Lower to Upper digit

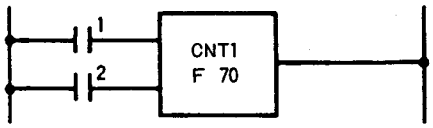
Program Example

(When a digital switch is connected to an I/O No. corresponding to FUN70)

- Timer external preset example (Input 1, TIM0, FUN70)

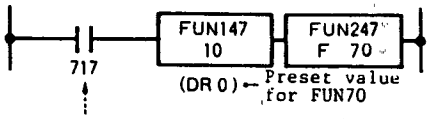


- Counter external preset example (Reset input 1, clock input 2, CNT1, FUN70)



- External preset example of counted value coincidence comparison instruction
  (Counter 30, Output 200, FUN70)

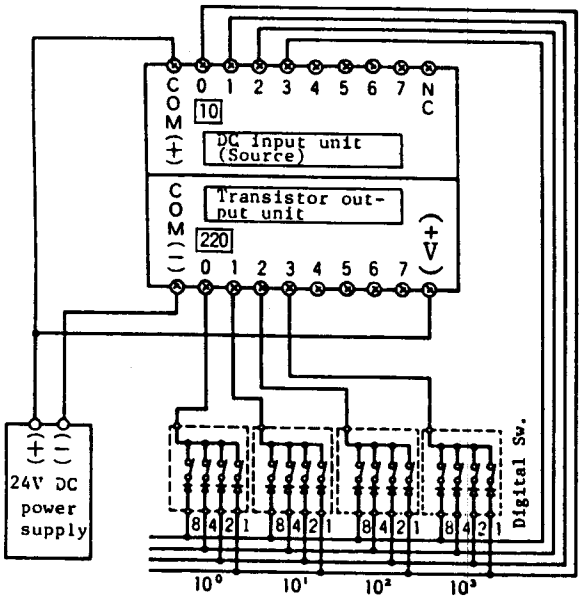
- Setting a constant for computing instruction



Note 1: Pulse input (SOT, etc.) cannot be used for this setting.

Note 2: Do not change preset values during counting. When a timer preset value is changed, the changed value becomes effective from the next timer operation.

Standard Connection Diagram (For the example at left)



Note 3: Initial input and output numbers are allocated via FUN30 and 31.

Note 4: When the external presetting (FUN70 to 85) is used, a program requires a scan time of 15msec at minimum.

Note 5: When changing a preset value via an external preset device (digital switch), it takes a maximum of 15 scan times to register the changed value correctly.

Note 6: When the external presetting is used as an operand of a computing instruction, be sure to use a continuous ON input for the conditions of the instruction. A value is read correctly 10 to 15 scans after turning ON the input.

Note 7: External presetting cannot be used in an MCS or JMP instruction.

External Display Function

Values of timers (TIM), counters (CNT) and data registers (DR) can be displayed on external digital display devices using a standard transistor output unit.

Specifications

Display system	Dynamic lighting display
No. of circuits	Max. 8 (BCD 4 digits)
No. of outputs	Transistor output 8 points/circuit (Digit selection: 4 points, BCD output: 4 points)
Applicable display unit	7-segment LED digital display: BCD input (negative logic) with latch 24V DC (Ex.) IDEC's type · DD33-F31N-B(Z) · DD96-F(R)31N-B Note: Digit selection (latch) output can be latched to Low or High via FUN35.

Note 1: Be sure to use continuous ON input for input of external display instruction conditions. A correct value is displayed 8 scans after turning ON the input.

Note 2: External display instructions cannot be used more than 8 times.

Note 3: External display instruction cannot be used between MCS and MCR or between JMP and JEND.

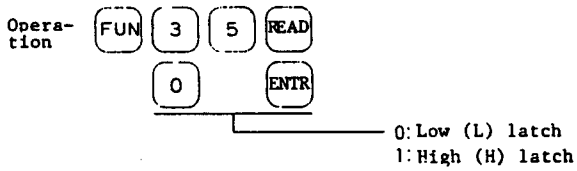
Program Example

External display instruction FUN147 25

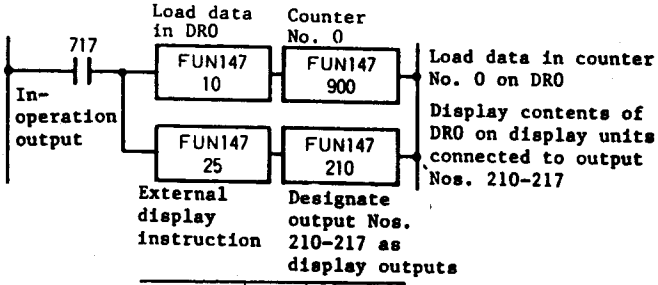
Converts data at data register DR0 into BCD and outputs display data by one digit after each scan. It takes 8 scans to output 4-digit display data.

Ex. To display the counted value of counter No. 0 on 4-digit 7-segment display units connected to output Nos. 210 to 217.

① Set latch conditions of external display instruction via function setting (FUN35).

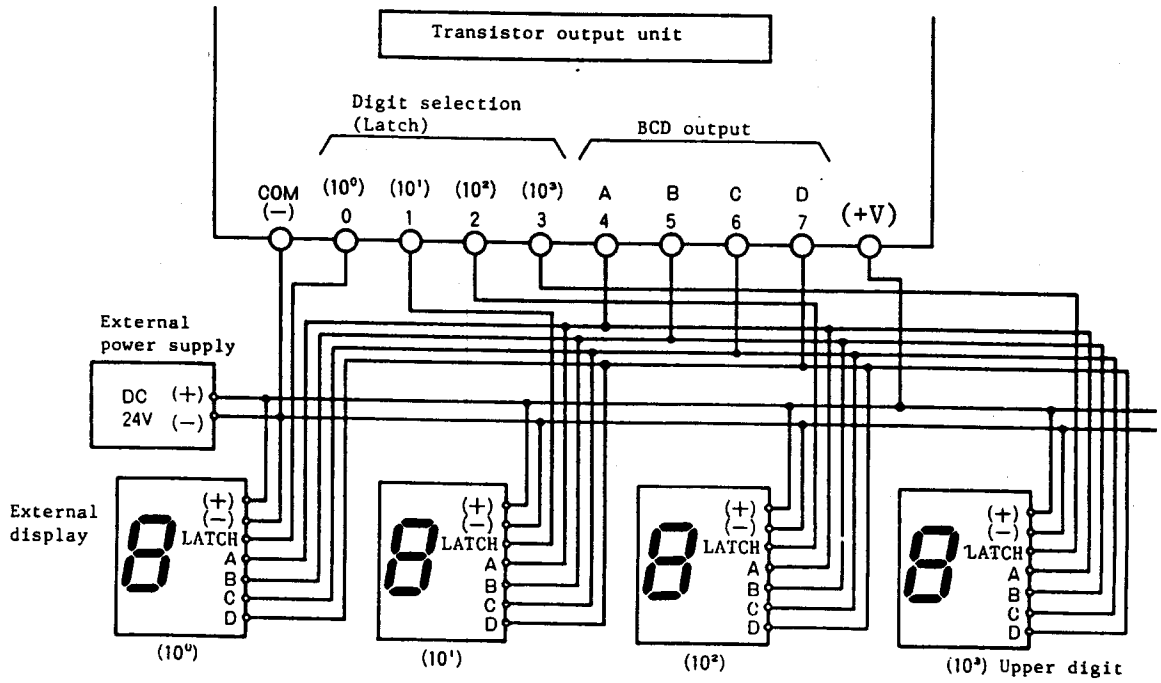


② Program



Address	Inst'n Word	Data
0	LOD	717
1	FUN	147
2		10
3	FUN	147
4		900
5	FUN	147
6		25
7	FUN	147
8		210

Standard Connection Diagram



Computing Function

The FA-1J has the following computing functions.

(1) Addition, (2) Subtraction, (3) Multiplication, (4) Division,
(5) BCD-to-binary convertion, (6) Binary-to-BCD convertion,
(7) Numerical value comparison (4-digit comparison)

Terms

Data (contents) of operand, data register or carry are shown in parentheses.

Example: When data register No. 10 contains data "5555";

Diagram = FUN147 / 810

Operand = Data register No. 10 = DR10

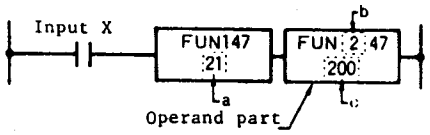
(Operand 810) = Contents of data resister No. 10 = (DR10) = 5555

Operand number = No. 810

Computing Instruction Composition

Two instructions are always used in pairs: Operation is designated by the code of FUN147 and 247 (computing instruction), and the next instruction gives an operand (information).

- For all computing instructions, data registers 0 and 1 (DR0 and DR1) are used.
- A data register is composed of 16 bits (2 bytes).



(1) Input X: 1 (ON) .... Computing is executed.
0 (OFF) ... Computing is not executed.

(2) a ... Designates the type of computing. (Table 2)
(Load, Store, Add, Subtract, Multiply, Divide, Compare, Display)

(3) b = "1" ... Designates I/O, IR, CNT, TIM, or DR.
b = "2" ... Designates a constant or external presetting.

(4) c ... Operand number or constant (Table 1)

Note: The second instruction FUN147 or FUN247 is not needed for a binary-to-BCD or BCD-to-binary conversion.

Operand List (Table 1)

Operand No. (c)	Operand Contents	
0- 60	Input	No. 0-157
200- 260	Output	No. 200-357
400- 680	Internal relay	No. 400-680
* 800- 899	Data register	No. 0- 99
900- 946	Counter	No. 0- 46
1000-1079	Timer	No. 0- 79

*All data registers are maintained during power failure.

Note 1: When TIM or CNT is the operand of a data store instruction, the data is stored in the T/C preset value area. For other than data store instructions, data of T/C present value becomes the object.

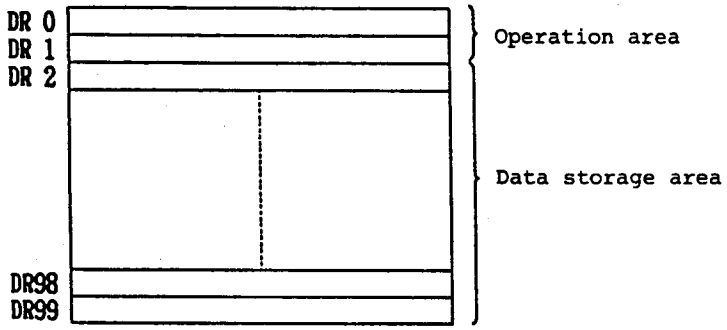
Note 2: When a data store instruction is executed for TIM or CNT, T/C preset value change IR (IR716) turns ON. The result is the same as T/C preset value change via program loader.

Note 3: Data store cannot be executed at T/C present value via computing instruction.

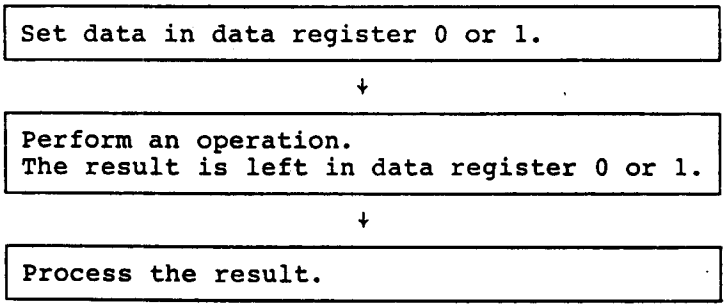
Note 4: Since the computing instruction is executed at each scan while input X is ON, use SOT instructions as required. If special internal relay 704 or 717 is used for an SOT instruction, the SOT output does not turn ON.

Basic Concept of Computing Instruction

- Data registers (DR0 to DR99) are used for the computing operation.

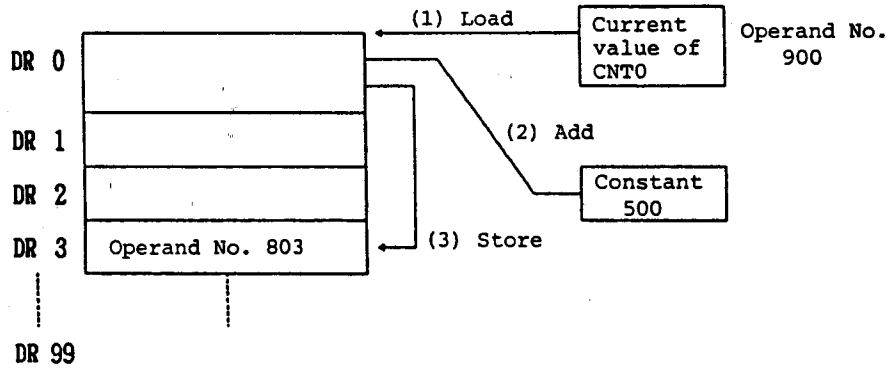


- Operational flowchart

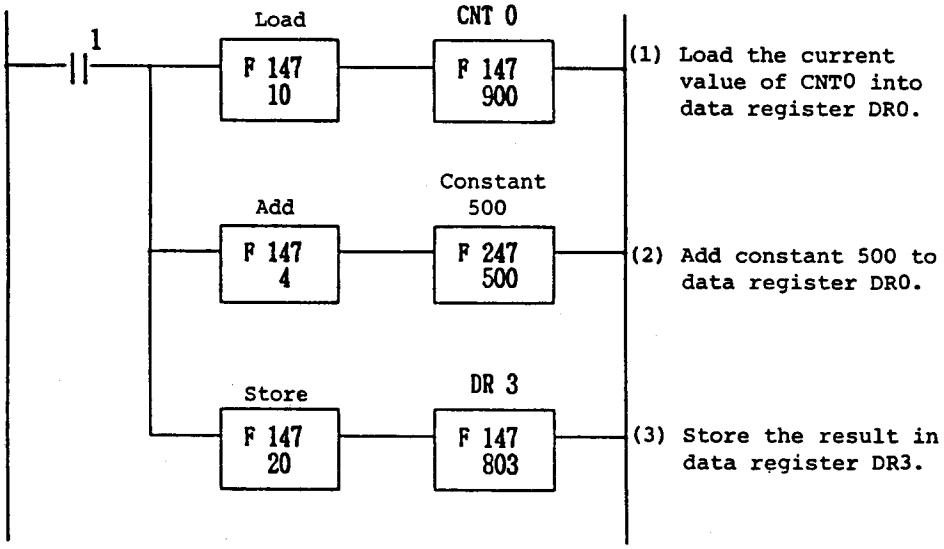


Basic Example Using Add Instruction

(Ex.) When input 1 is ON, constant 500 is added to the current value of CNT0 and the result is stored in data register DR3.



(Instruction word)



Operation Instruction List (Table 2)

DR: Data register (0-99)
CY: Carry

Note: (Operand) stands for data designaged by operand.

Instruction Type	Computing Instruction FUN 147 (a)	Function	Objects That Can be Designated by Operand	Forbidden Designation (Results in error 80)
	FUN 147 0	NOP	—	
Binary conversion BCD → BIN	FUN 147 1	Converts BCD value of DR 0 into binary and sets the result to DR 0.	—	
BCD conversion BIN → BCD	FUN 147 2	Converts binary value of DR 0 into BCD and sets the result to DR 0.	—	
4-digit comparison	FUN 147 3 Operand FUN047 0000	(DR 0) $\gtrless$ (Operand) Sets the result at internal relay: $>$ → 710, $=$ → 711, $<$ → 712	Timer, counter, data register, constant	
Addition (+)	FUN 147 4 Operand FUN047 0000	(DR 0) + (Operand) + (CY) → (DR 0), (CY)	Timer, counter, data register, constant	
Subtraction (−)	FUN 147 5 Operand FUN047 0000	(DR 0) − (Operand) − (CY) → (DR 0), (CY)	Timer, counter data register, constant	
Multiplication (x)	FUN 147 6 Operand FUN047 0000	(DR 0) x (Operand) → (DR 1), (DR0) (Upper & lower 4 digits)	Timer, counter, data register, constant	
Division (÷)	FUN 147 7 Operand FUN047 0000	(DR 0) − (Operand) → (DR 1), (DR0) (Remainder) (Quotient)	Timer, counter, data register, constant	
Data register data shift	FUN 147 8 Operand FUN047 0000	→(DR m) → (DR m+1) ····· → (DR n) ····· Designated number only	Data register	Anything other than data register
BCD digit left shift	FUN 147 9 Operand FUN047 0000	Left shift of (DR1) and (DR0) by the number of digits (operand) (Lower digits are set to 0.)	Data register, constant	
Data load (16-bit)	FUN 147 10 Operand FUN047 0000	(DR 0) ← (Operand)	I/O, internal relay, SFR, timer, counter, data register, constant	
Data load (8-bit)	FUN 147 11 Operand FUN047 0000	(DR 0) ← (Operand) 8-bit Upper 8 bits of DR0 are set to 0.	I/O, internal relay, SFR	
Data load (Indirect)	FUN 147 12 Operand FUN047 0000	(DR 0) ← (Operand + (DR 1))	Timer, counter data register	Anything other than those listed at left
Data load (16 bit)	FUN 147 13 Operand FUN047 0000	(DR 1) ← (Operand)	I/O, internal relay, SFR, timer, counter, data register, constant	
Data load (8-bit)	FUN 147 14 Operand FUN047 0000	(DR 1) ← (Operand) 8-bit Upper 8 bits of DR1 are set to 0.	I/O, internal relay, SFR	
Data increment	FUN 147 18 Operand FUN047 0000	(Operand) ← (Operand) + 1	Data register	Anything other than those listed at left
Data decrement	FUN 147 19 Operand FUN047 0000	(Operand) ← (Operand) − 1	Data register	Anything other than those listed at left
Data store (16-bit)	FUN 147 20 Operand FUN047 0000	(DR 0) → (Operand)	Output, internal relay, SFR, timer, counter, data register	Constant
Data store (8-bit)	FUN 147 21 Operand FUN047 0000	(DR 0) → (Operand) 8-bit	Output, internal relay, SFR	Constant
Data store (Indirect)	FUN 147 22 Operand FUN047 0000	(DR 0) → (Operand + (DR 1))	Counter, timer, data register	Anything other than those listed at left
Data store (16-bit)	FUN 147 23 Operand FUN047 0000	(DR 1) → (Operand)	Output, internal relay, SFR, timer, counter, data register	Constant
Data store (8-bit)	FUN 147 24 Operand FUN047 0000	(DR 1) → (Operand) 8-bit	Output, internal relay, SFR	Constant
Data display (Dynamic)	FUN 147 25 Operand FUN047 0000	Converts (DR0) into BCD and gives display output after every scan.	Output	Anything other than output

Note: As DR0 and 1 are used for computing operation, do not use them for data store in user's programs.

Computing Instruction

BCD-to-Binary Conversion

Basic

- Converts the contents of DRO from BCD into binary when input is turned ON, and sets the result again at DRO.

Operand ..... None

Binary-to-BCD Conversion

Basic

- Converts the contents of DRO from binary into BCD (4-digit) when input is turned ON, and sets the result again at DRO.

Operand ..... None

Supplementary

- Numerical value: BCD (0-9999) to binary (0-270F) (hexadecimal)
- Numerical value error judgment: Error results when the value of a digit exceeds (0A) (hexadecimal)
- When a BCD signal is read via FUN70 to FUN85, BCD-to-binary conversion is executed automatically. When BCD data is read in other way from outside, the next operation cannot be executed without executing this binary conversion.

Supplementary

- Numerical value: Binary (0-270F) (hexadecimal) to BCD (0-9999)
- Numerical value error judgment: Error results when 16-bit binary value > (270F) (hexadecimal) Conversion is not executed in the event of error.
- This conversion needs to be executed when data (binary value) of timer and counter are outputted as BCD output.

Note: The following computing instructions are executed in binary values:

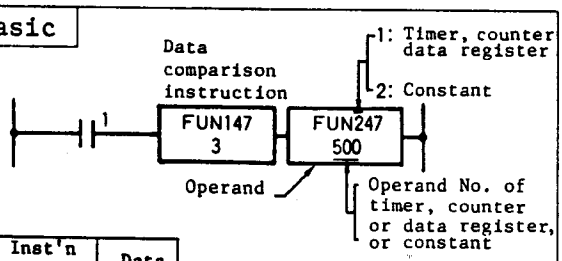
Addition, subtraction, multiplication, division, data increment, data decrement, and data display

The range of all binary values is (0 to 270F)H.

Data Comparison (4-Digit)

FUN147
3

Basic



Inst'n Word	Data
LOD	1
FUN	147
	3
FUN	247
	500

- A data comparison instruction is always used in combination with an operand.
- Compares data designated via operand (hexadecimal) with those of DR0 when input is turned ON, and turns ON one among internal relays 710, 711 and 712 according to the result. The other two are turned OFF.

  When DR0 > Operand data, IR710 is turned ON
  When DR0 = Operand data, IR711 is turned ON
  When DR0 < Operand data, IR712 is turned ON

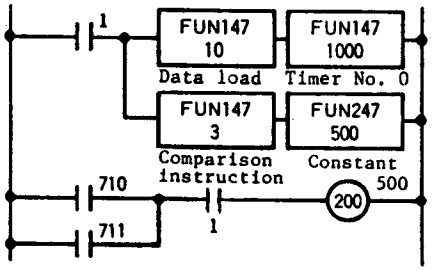
- When input is OFF, IR710 to IR712 remain unchanged.

Operand ..... TIM, CNT, DR, Constant

Supplementary

- Prior to execution of this computing instruction, an instruction to set compared data to DR0 must be executed.

(Ex.) When input 1 is ON, data of timer No. 0 is read out to DR0 and compared with constant 500 set by operand. When DR0 ≧ 500, output 200 is turned ON.

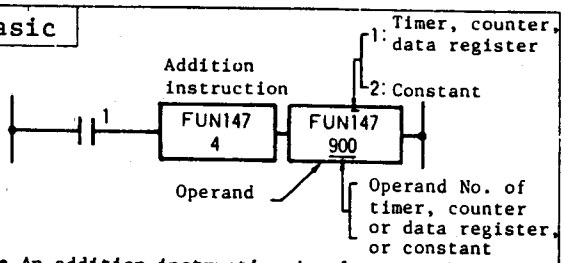


Note: Be sure to program an AND circuit with the contact for execution and comparison result 710, 711 and 712 contacts.

Addition

FUN147
4

Basic



- An addition instruction is always used in combination with an operand.
- Adds data designated via operand to DR0 and carry (IR707) when input is turned ON, and sets the result again at DR0 and carry (IR707).

  (DR0) + (Operand) + (CY) → (DR0) & (CY)
  Carry

Operand ..... TIM, CNT, DR, Constant

Supplementary

- Normal range of sum

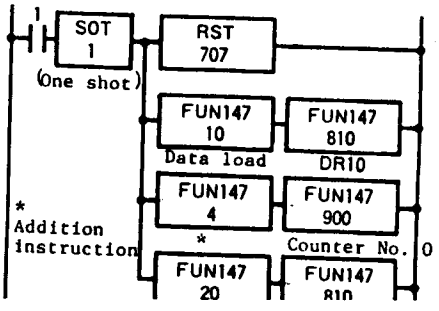
	(DR0)	(Operand)	(CY)		(CY)	(DR0)
min.	0	0	0	→	0	0
max.	9999	9999	1	→	1	9999

- Computing example

(DR0) + (Operand) + (CY)		(CY)	(DR0)
1 + 900 + 0	→	0	901
0 + 2000 + 1	→	0	2001
1000 + 9000 + 0	→	1	0000
9999 + 9999 + 1	→	1	9999

- Numerical value error is given when the sum including carry is 20000 or more.
- Prior to this computing instruction, data to be added must be set to DR0, and carry must also be reset if necessary.

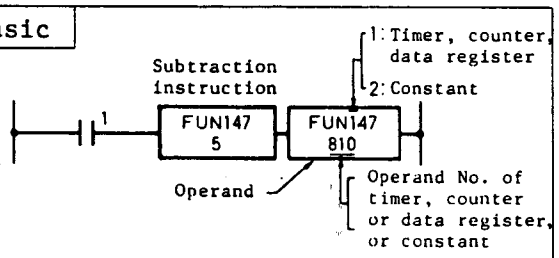
(Ex.) Data of DR10 is read out to DR0 via ON signal of input 1, and counted value of counter No. 0 is added and written again in DR10.



Subtraction

FUN147
5

Basic



- A subtraction instruction is always used in combination with an operand.
- Subtracts data designated via operand and borrow (IR707) from data of DR0 when input is turned ON, and sets the result at DR0 and borrow (IR707).

  (DR0)-(Operand)-(Borrow) → (DR0) & (Borrow)

Operand ..... TIM, CNT, DR, Constant

Supplementary

- Normal range of difference

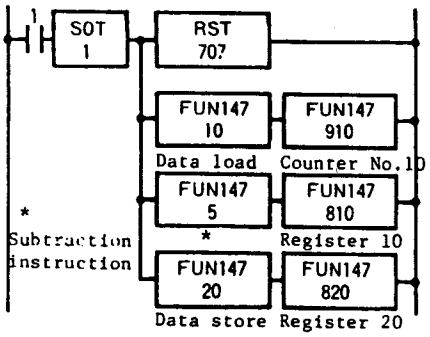
	(DR0)	Operand	(Borrow)		(Borrow)	(DR0)
min.	0	9999	1	→	1	0
max.	9999	0	0	→	0	9999

- Numerical value error is given when the result exceeds 9999 or is less than -10000.
- Computing Result (A negative value is indicated in its complement for 10000. To indicate an absolute value of a negative value, subtract the result from 0.)

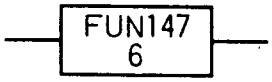
Numeral	(Borrow)	(DR0)
−10000	1	0000
− 9999	1	0001
− 9998	1	0002
⋮	⋮	⋮
− 2	1	9998
− 1	1	9999
0	0	0000
1	0	0001
⋮	⋮	⋮
9999	0	9999

- Prior to this computing, data to be subtracted must be set to DR, and borrow must also be reset if necessary.

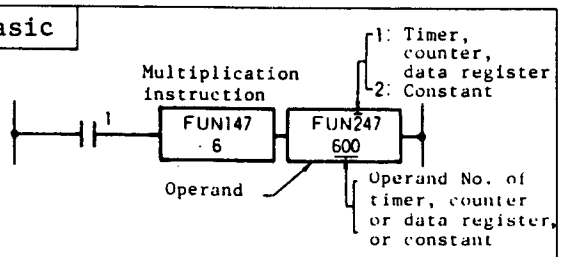
(Ex.) Data of counter No. 10 is read out to DR0 via ON signal of input 1, data of DR10 is subtracted, and the result is written in DR20.



Multiplication



Basic



- A multiplication instruction is always used in combination with an operand.
- Multiplies data of DR0 by data designated via operand when input is turned ON, and sets the result at DR0 and DR1.

(DR0) x (Operand) → (DR1) (DR0)
Upper 4 digits Lower 4 digits

Operand ..... TIM, CNT, DR, Constant

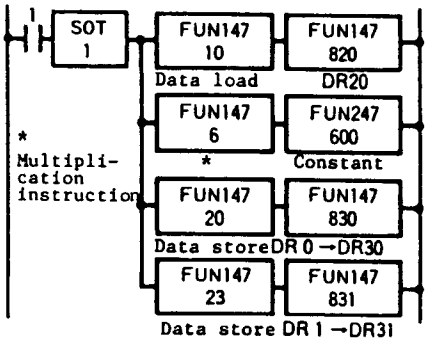
Supplementary

- Normal range of product

	(DR 0)	(Operand)		(DR 1)	(DR 0)
min.	0	0	→	0	0
max.	9999	9999	→	9998	0001

- Numerical value error is given when a multiplier or multiplicand exceeds 9999.
- Prior to this computing instruction, multiplicand must be set to DR0.
- When the result is less than 10000 or (2710)H, the result is set at DR0 and 0 is set at DR1.
- When the result is more than 9999 or (270F)H, the result is set at DR1 as upper digits.

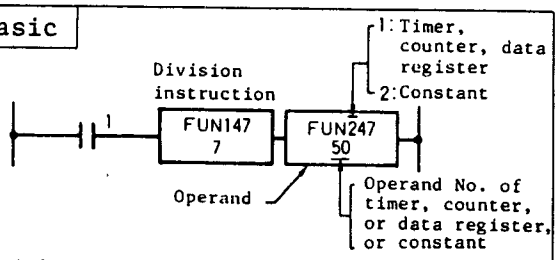
(Ex.) Data of DR20 is read out to DR0 when input 1 is turned ON. This data is multiplied by constant 600 designated via operand, and data of DR0 (BCD lower 4 digits) are written in DR30 and data of DR1 (BCD upper 4 digits) in DR31.



Division

FUN147
7

Basic



- A division instruction is always used in combination with an operand.
- Divides data of DR0 by data designated via operand when input is turned ON and sets the quotient at DR0 and the remainder at DR1.

(DR0) ÷ (Operand) → (DR0) .... (DR1)
Quotient Remainder

Operand ..... TIM, CNT, DR, Constant

Supplementary

- Normal range of quotient

Quotient (DR0)	0 to 9999
Remainder (DR1)	0 to Divisor - 1

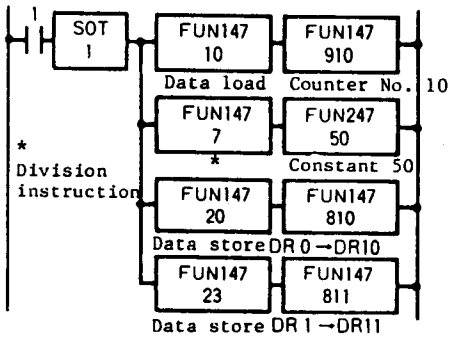
- Numerical value error is given when;
  - Divisor is 0.
  - Divisor or dividend exceeds 9999.
- Computing example

(DR0) ÷ (Operand)		Quotient (DR0)	Remainder (DR1)
1000 ÷ 50	→	20	0
9 ÷ 2	→	4	1
2 ÷ 9	→	0	2

Note: When (DR0) is smaller than the (Operand), the quotient is 0 and the original data of DR0 becomes the remainder.

- Prior to this computing, data must be set at DR0 as a dividend.

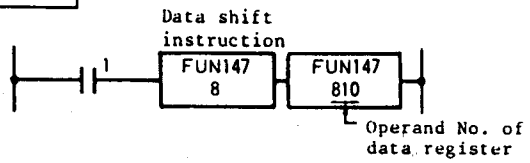
(Ex.) Data of counter No. 10 is read out to DR0 when input 1 is turned ON. This data is divided by constant 50 designated via operand, and data of DR0 (quotient) and DR1 (remainder) are written in DR10 and DR11 respectively.



Data Shift

FUN147
8

Basic



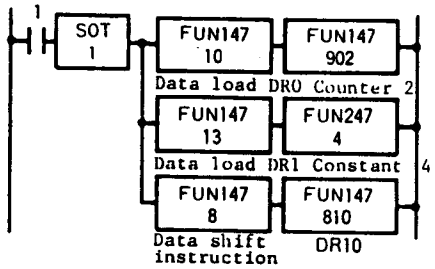
- A data shift instruction is always used in combination with an operand.
- Shifts data of data registers whose numbers are designated via DR1, starting from a data register designated via operand.
- Designated data
  (1) Data designated via operand: Data register number to start shifting.
  (2) Data of DR0: Input data
  (3) Data of DR1: The number of data registers to be shifted.

Operand ..... DR

Supplementary

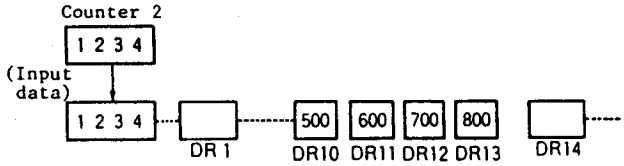
- Prior to execution of this instruction, data must be set to DR0 and 1.

(Ex.) When input 1 is turned ON, input data read to DR0 from counter 2 is set to DR10. Then, data of four data registers DR10, 11, 12 and 13 are shifted to the next data register respectively.

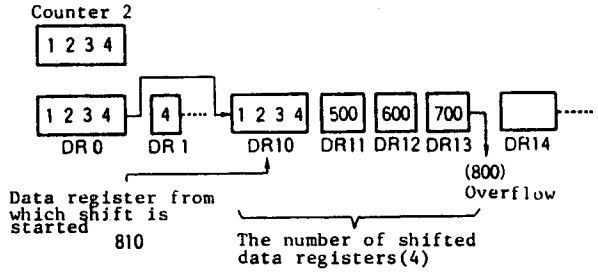


- Data movement

Prior to computing execution



After computing execution



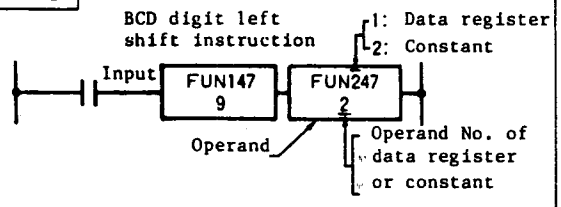
- Numerical value error judgment is given when:

  (Operand) + (DR1) > 900

BCD Digit Left Shift

FUN147
9

Basic



- A BCD digit left shift instruction is always used in combination with an operand.
- Shifts a total of BCD 8 digits including BCD upper 4 digits in DR1 and lower 4 digits in DR0 to the left by a number designated via operand. Lower digits are set to 0.
- The result remains in DR1 and DR0.
- Effective range of operand contents: 1 to 7

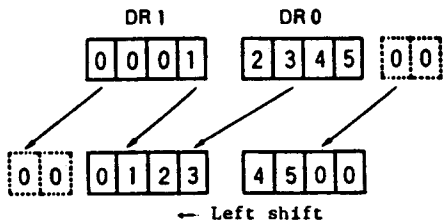
Operand ..... DR, Constant

Supplementary

- Numerical value error judgment is given when:
  ① The value designated via operand exceeds 7.
  ② Contents of DR1 and 0 are not BCD.
- This operation is effective to set the effective number of digits for multiplication or division data.

(Ex.) When input 1 is turned ON, data of (DR1) = 0001 and (DR0) = 2345 are shifted to the left by two.

- Data movement

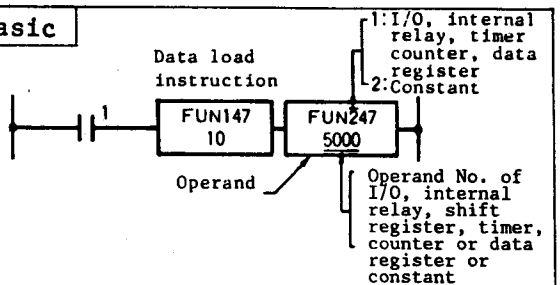


Note: Binary data is processed by this instruction.

Data Load (16-Bit Data)

FUN147
10

Basic



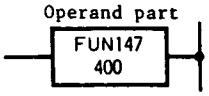
- A data load instruction is always used in combination with an operand.
- Sets data designated via operand at DR0 when input is turned ON.
- (Operand) 16-bit data → (DR0)

Operand .....

Supplementary

- When an input, output or internal relay is designated as an operand for this instruction, 16 points of input, output or internal relay data are read continuously starting from a designated number.

(Ex.)

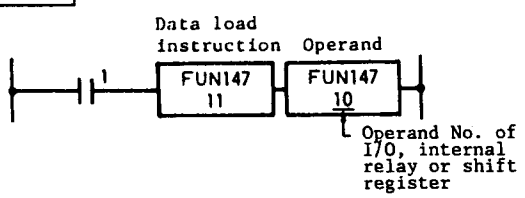


In this case, data of internal relay Nos. 400 to 407 and 410 to 417 are read. No. 400 is the LSB (least significant bit) and No. 417 is the MSB (most significant bit).

Data Load (8-Bit Data)

FUN147
11

Basic



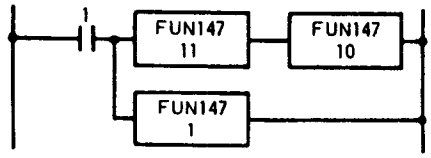
- A data load instruction is always used in combination with an operand.
- Sets 8-bit data of input, output or internal relay designated via operand at lower 8-bits of DR0 when input is turned ON.
- (Operand) 8-bit data → (DR0)

Operand ..... IN, OUT, IR, SFR

Supplementary

- 8 points of input, output or internal relay data are read starting from the number designated via this instruction.
  In this example, data of input Nos. 10 to 17 are read. (No. 10 is the LSB.)
- Upper 8 bits of DR0 are set to 0.
- This instruction can be programmed in combination with FUN147 1

(Ex.)

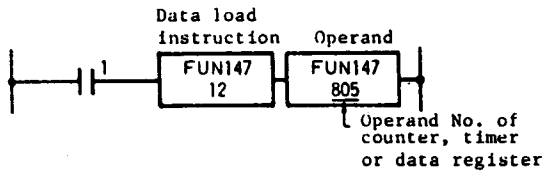


When input is turned ON, 8-bit BCD data of input Nos. 10 to 17 are read, converted into BIN (binary) values and set at DR0.

Data Load (Indirect 16-Bit Data)

FUN147
12

Basic



- A data load instruction is always used in combination with an operand.
- Adds the contents of DR1 to the operand number designated via an operand (in this example, No. 805 stands for DR5) and sets the contents of the operand at DR0 when input is turned ON.
- (Operand No. + (DR1)) → (DR0)

Operand ..... TIM, CNT, DR

Supplementary

- Operation via the above instruction

  ① When the following data are contained in data registers prior to execution:

Data register	Name	(DR0)	(DR1)	(DR5)	(DR15)
	Operand No.	800	801	805	815
Data		0	10	7	50

  ② Execution process is:
  (Operand No. + (DR1)) = (805 + 10) = (815) = (DR15) → (DR0)

  ③ Values of data registers are changed as follows after execution.

Data register	(DR0)	(DR1)	(DR5)	(DR15)
Data	50	10	7	50

Note: Note that "Operand No. +(DR1)" is not the same as "(Operand) + (DR1) = (DR5) + (DR1) = 7 + 10".

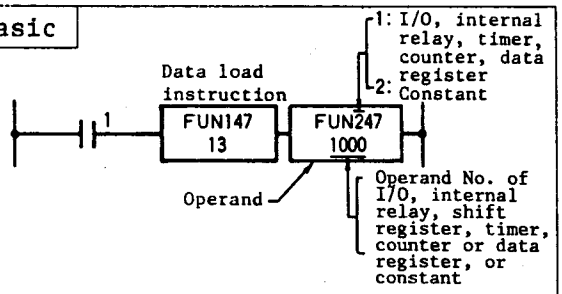
- This instruction is used to extract data (the nth data in data arrangement).
- Numerical value error judgment is given when:

  Operand No. +(DR1) > the maximum No. of the operand

Data Load (16-Bit Data)

FUN147
13

Basic



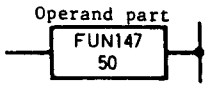
- A data load instruction is always used in combination with an operand.
- Sets data designated via operand at DR1 when input is turned ON
- (Operand) 16-bit data → (DR1)

Operand ..... IN, OUT, IR, SFR, TIM, CNT, DR, Constant

Supplementary

- 16 points of input, output or internal relay data are read continuously starting from the designated number when an input, output or internal relay is designated as an operand via this instruction.

(Ex.)

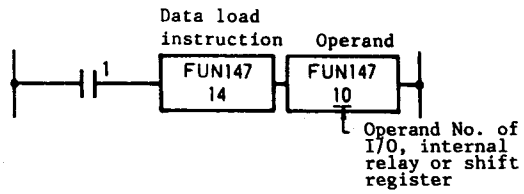


In this case, data of input Nos. 50 to 57 and 60 to 67 are read.
50 is LSB (Least significant bit)
67 is MSB (Most significant bit)

Data Load (8-Bit Data)

FUN147
14

Basic



- A data load instruction is always used in combination with an operand.
- Sets 8-bit data of input, output or internal relay designated via operand at lower 8 bits of DR1 when input is turned ON.
- (Operand) 8-bit data → (DR1)

Operand ..... IN, OUT, IR, SFR

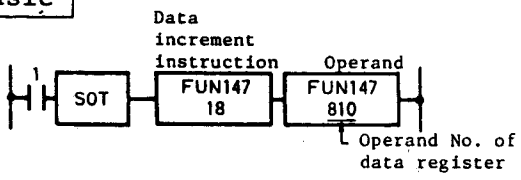
Supplementary

- 8 points of input, output or internal relay data are read continuously starting from the number designated via this instruction.
  In this example, data of input Nos. 10 to 17 are read.
- Upper 8 bits of DR1 are set to 0.

Data Increment

FUN147
18

Basic



- A data increment instruction is always used in combination with an operand.
- Adds one to data of the data register designated via operand and writes the result in the data register when input is turned ON.
- (Operand) + 1 → (Operand)

Operand ..... DR

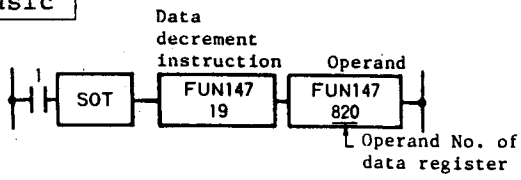
Supplementary

- Error (ERR80) is given during execution when anything other than data register is designated as an operand.
- During computing execution, data registers DR0 and 1 and carry CY (IR707) remain unchanged.
- Object data are 0 to 9999. If 9999 is increased by one, the result will be 0. In this case also, carry (CY) will not be given.
- A numeral (2710) (hexadecimal) or more, if set, will not lead to a numerical value error, but if it is increased by one, the result will be 0.

Data Decrement

FUN147
19

Basic



- A data decrement instruction is always used in combination with an operand.
- Subtracts one from data of the data register designated via operand and writes the result in the data register when input is turned ON.
- (Operand) - 1 → (Operand)

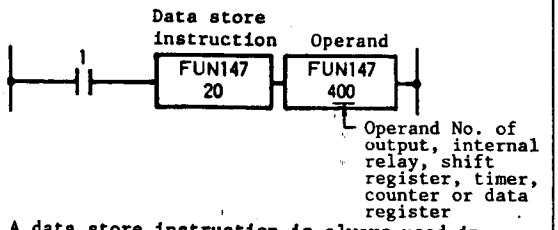
Operand ..... DR

Supplementary

- Error (ERR80) is given during execution when anything other than data register is designated as an operand.
- Data registers DR0 and 1 and carry CY (IR707) remain unchanged during computing execution.
- Object data are 0 to 9999. If 0 is decreased by one, the result will be 9999, and carry CY will not be given.

Data Store (16-Bit Data)

Basic

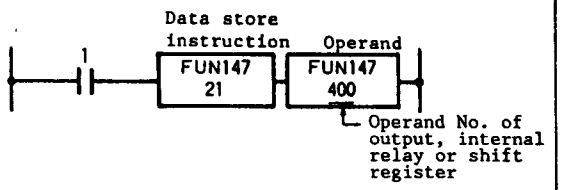


- A data store instruction is always used in combination with an operand.
- Sets data of DRO at the location designated via operand when input is turned ON.
- (DRO) → (Operand) 16-bit data

Operand ..... OUT, IR, SFR, TIM, CNT, DR

Data Store (8-Bit Data)

Basic

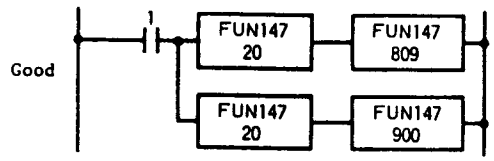


- A data store instruction is always used in combination with an operand.
- Sets lower 8-bit data of DRO at output or internal relay designated via operand when input is turned ON.
- (DRO) → (Operand) 8-bit data

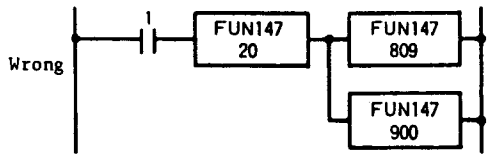
Operand ..... OUR, IR, SFR

Supplementary

- When output or internal relay is designated as an operand via this instruction, 16 points of outputs or internal relays are occupied continuously starting from the designated number. In this example, internal relay Nos. 400 to 407 and 410 to 417 are automatically occupied. No. 400 is the LSB and No. 417 is the MSB. For timer, counter or data register, data is set to the designated point.
- Data store at two or more locations simultaneously.



The following is an error.



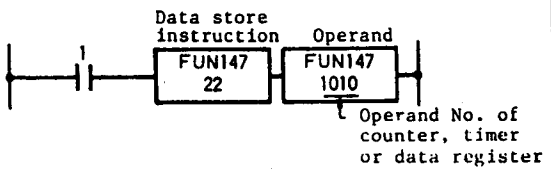
Supplementary

- When this instruction is used, 8 points of outputs or internal relays are continuously occupied starting from the designated number. In this example, internal relay Nos. 400 to 407 are automatically occupied. No. 400 is the LSB.

Data Store (Indirect 16-Bit Data)

FUN147
22

Basic



- A data store instruction is always used in combination with an operand.
- Sets data of DR0 at the location calculated by adding the operand number designated via operand (in this case, No. 1010 corresponds to TIM10) to the contents of DR1 when input is turned ON.
- (DR0) → (Operand No. + (DR1))

Operand ..... TIM, CNT, DR

Supplementary

- Operation via the instruction shown above

① When each data register and timer has the following values prior to execution;

Data register	Name	(DR0)	(DR1)	(TIM10)	(TIM13)
	Operand No.	800	801	1010	1013
Data		345	3	178	255

② Execution process is:
(DR0) → (Operand No. + (DR1))
= (1010 + 3) = (1013) = (TIM13)

③ After execution

Data register, etc.	(DR0)	(DR1)	(TIM10)	(TIM13)
Data	345	3	178	345

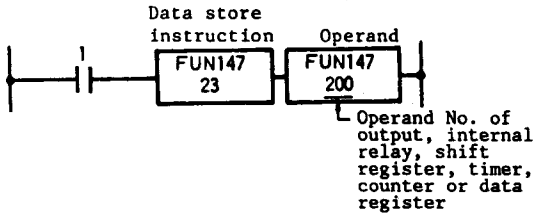
Note: Note that "Operand No. + (DR1)" is not the same as "(Operand) + (DR1) = (TIM10) + (DR1) = 178 + 3".

- This instruction is used for data distribution (storage of data at the nth location in data arrangement).
- Numerical value error judgement is given when: Operand No. + (DR1) > the maximum number of the operand

Data Store (16-Bit Data)

FUN147
23

Basic

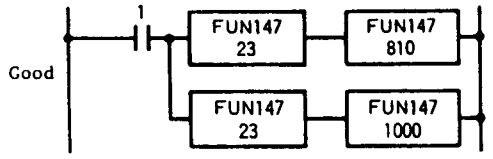


- A data store instruction is always used in combination with an operand.
- Sets data of DR1 at the location designated via operand when input is turned ON.
- (DR1) → (Operand) 16-bit data

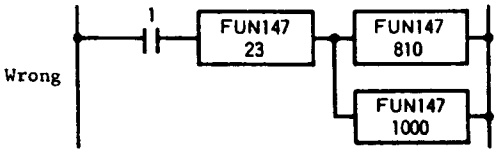
Operand ..... OUT, IR, SFR, TIM, CNT, DR

Supplementary

- When output or internal relay is designated as an operand via this instruction, 16 points of outputs or internal relays are occupied continuously starting from the designated number. In this example, input relay Nos. 200 to 207 and 210 to 217 are automatically occupied.
For timer, counter and data register, data is set to the designated point.
- Data store at two or more locations simultaneously.



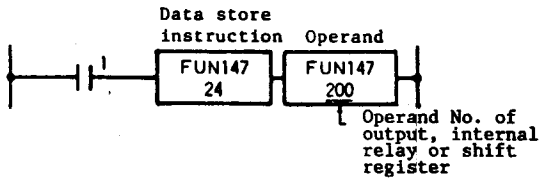
The following is an error.



Data Store (8-Bit Data)

FUN147
24

Basic



- A data store instruction is always used in combination with an operand.
- Sets lower 8-bit data of DR1 at output or internal relay designated via operand when input is turned ON.
- (DR1) → (Operand) 8-bit data

Operand ..... OUT, IR, SFR

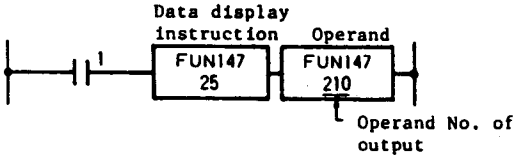
Supplementary

- When this instruction is used, 8 points of outputs or internal relays are occupied continuously starting from the designated number.
  In this example, input Nos. 200 to 207 are automatically occupied.
  No. 200 is the LSB.

Data Display (Dynamic Display)

FUN147
25

Basic



- A data display instruction is always used in combination with an operand.
- Sets data of DR0 at the output designated via operand as display output when input is turned ON.

Operand ..... OUT

Supplementary

- As 2 scans are required to display one digit, 8 scans are required to display four digits.
- When this instruction is used, 8 points of outputs are occupied continuously starting from the designated output number.
  In this example, output Nos. 210 to 217 are automatically occupied.
- This instruction cannot be used more than 8 times.
- This instruction cannot be used between JMP and JEND and between MCS and MCR.

Instruction Execution Time

Instruction Word	Operand	Max.Time (μsec)
END		3600
LOD	IN, OUT, IR	30
AND	IN, OUT, IR	28
OR	IN, OUT, IR	28
OUT	OUT, IR	30
SET	SFR, OUT, IR	31
RST	SFR, OUT, IR	31
LOD N	IN, OUT, IR	31
AND N	IN, OUT, IR	28
OR N	IN, OUT, IR	28
LOD	T	45
LOD	C	48
LOD	R	40
OR LOD		26
AND LOD		26
SOT		44
MCS		27
MCR		43
JMP		27
JEND		27

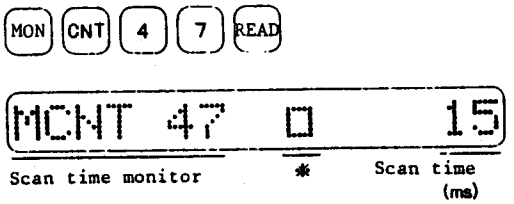
Inst'n Word	Number etc.	Max.Time (μsec)	Ave.Time (μsec)
TIM	0-79	131	96
CNT	0-44	133	117
CNT	45-46	122	106
SFR(N)	n bits	83+12×n	74
TIM F		230	42
CNT F		230	42
FUN 100		80	
FUN 200		78	
FUN 300		38	

Instruction Word	Time
Any computing instruction (with operand)	Approx. 200 μsec

Scan Time Monitor Function

In an FA-1J unit, scan time can be read via monitor function.

- Operating procedure



* Display marked with * is irrelevant.

- The above scan time does not include the response delay in the I/O unit. When calculating the actual I/O response time, add the response delay to the above scan time.
- The scan time includes an inherent scan time (approx. 4 msec) for every scanning.

FA-1J PROGRAMMING SHEET

Sheet No. | of

Step (Address)	Instruction Word	Number Data	Remarks	Step (Address)	Instruction Word	Number Data	Remarks
0				50			
1				51			
2				52			
3				53			
4				54			
5				55			
6				56			
7				57			
8				58			
9				59			
10				60			
11				61			
12				62			
13				63			
14				64			
15				65			
16				66			
17				67			
18				68			
19				69			
20				70			
21				71			
22				72			
23				73			
24				74			
25				75			
26				76			
27				77			
28				78			
29				79			
30				80			
31				81			
32				82			
33				83			
34				84			
35				85			
36				86			
37				87			
38				88			
39				89			
40				90			
41				91			
42				92			
43				93			
44				94			
45				95			
46				96			
47				97			
48				98			
49				99			

Title				Approved by	Checked by	Designed by
Program name						
Date		Dwg. No.				

	Allocation Table	Description		

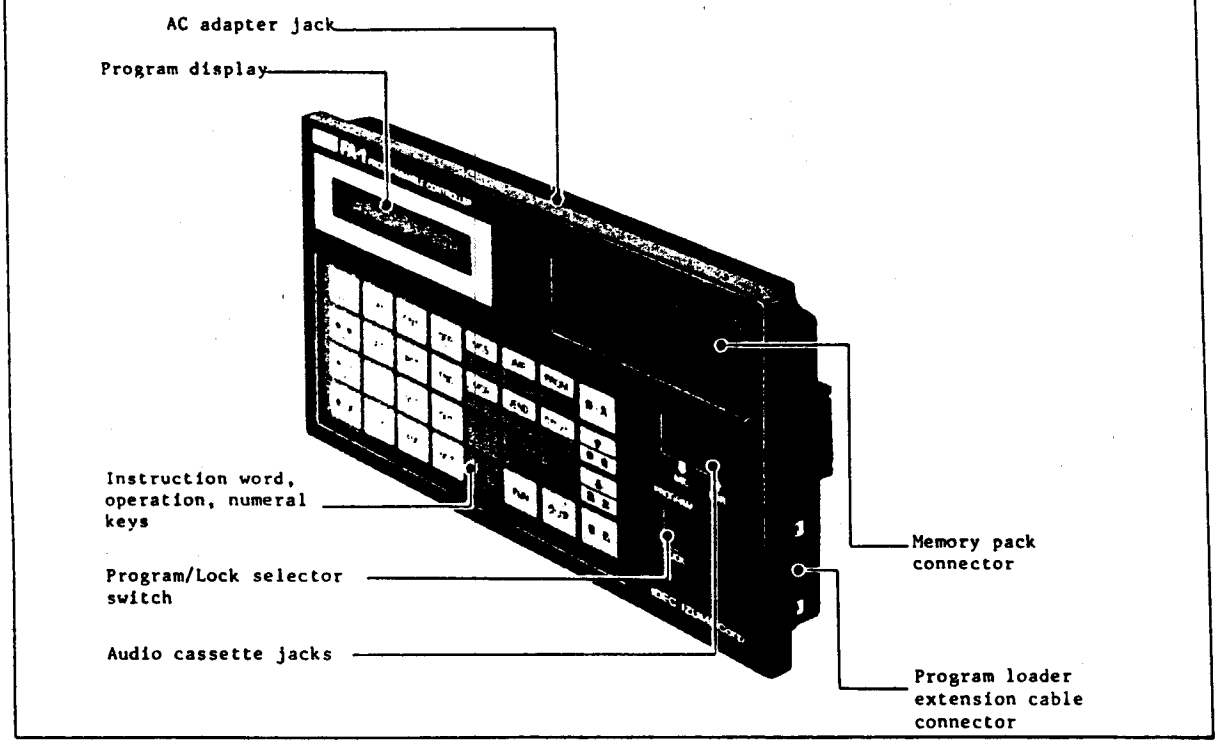
No.	Symbol . Description	Remarks	No.	Symbol . Description	Remarks
0			0		
1			1		
2			2		
3			3		
4			4		
5			5		
6			6		
7			7		
0			0		
1			1		
2			2		
3			3		
4			4		
5			5		
6			6		
7			7		
0			0		
1			1		
2			2		
3			3		
4			4		
5			5		
6			6		
7			7		
0			0		
1			1		
2			2		
3			3		
4			4		
5			5		
6			6		
7			7		

Approved by
Checked by
Designed by

Chapter 3 — PROGRAM LOADER

Program Loader

Part Description



Type and Program Capacity

Type	Program Capacity
PFA-1H401RE	For 1K steps
PFA-1H404RE	For 4K steps

Note: 964 steps maximum for 1K steps
4,036 steps maximum for 4K steps

- **Program capacity**

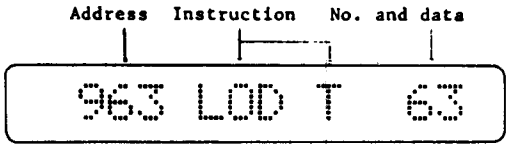
Program capacity by combination with the program loader and memory pack.

Memory Pack / Loader	CMOS-RAM		EPROM	E^2PROM
	PFA-1M21 (1K)	PFA-1M24 (4K)	PFA-1M34 (4K)	PFA-1M14 (4K)
PFA-1H401RE (1K steps)	1K steps	1K steps	1K steps	1K steps
PFA-1H404RE (4K steps)	1K steps	4K steps	4K steps	4K steps

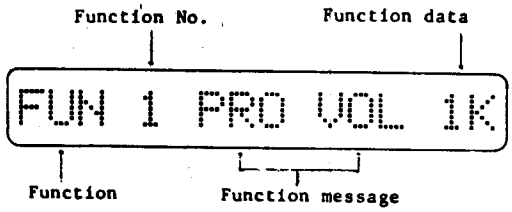
* A 4K-step memory pack can also be used for 1K steps.

Sample Display

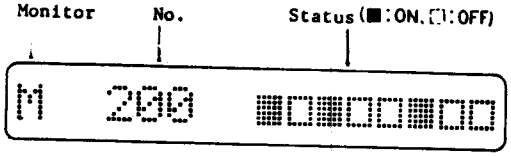
- Program display



- FUN (Function) display



- Monitor display

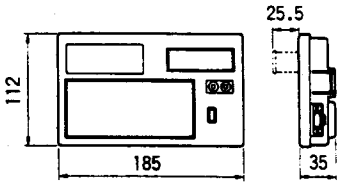


- Message display

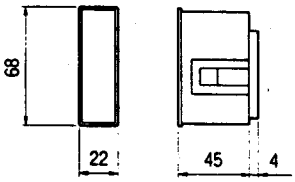
(Is PROM writing OK?)

Dimensions

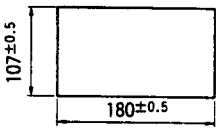
- Program Loader



- Memory Pack



(Panel Cut-Out for Program Loader)



Panel thickness: 1.0 to 4.0

For mounting the program loader on a panel surface, see page 41.

Supplementary

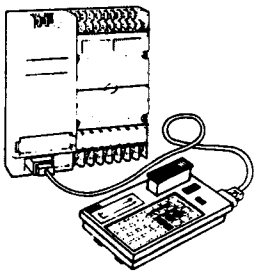
1. The program loader incorporates a 1K- or 4K-step CMOS-RAM memory, which is backed up by a super capacitor.
   The capacitor's back-up period is approx. one week.

Programming Procedures & Precautions

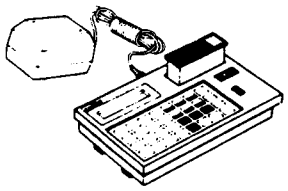
Power ON

- The program loader can be powered in two ways:

1) Connect the CPU unit to the loader, using a loader extension cable, and supply power from the CPU unit.



2) Connect an AC adapter to the loader to supply power.

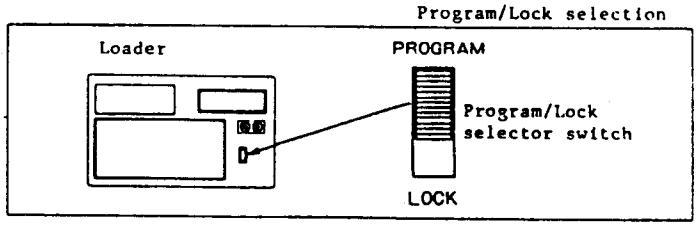


- In either case, when power is turned ON, a short tone (beep) is generated, displaying address 0.
- When programming, it is not necessary to install a memory pack in the program loader.

Explanation

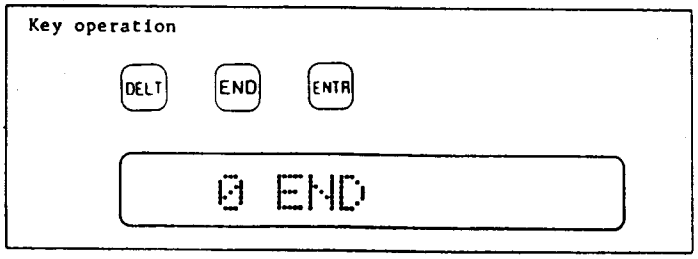
Move the Program/Lock selector switch to PROGRAM.

Program/Lock selection



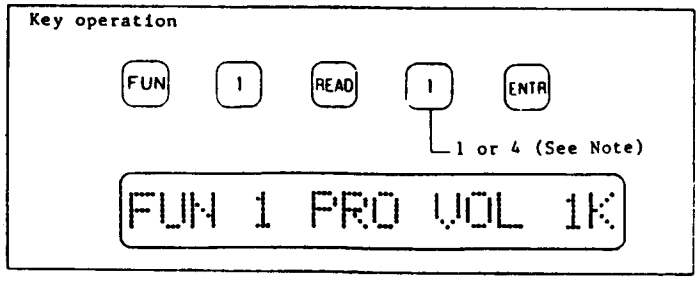
Clear all programs within the loader.

Key operation



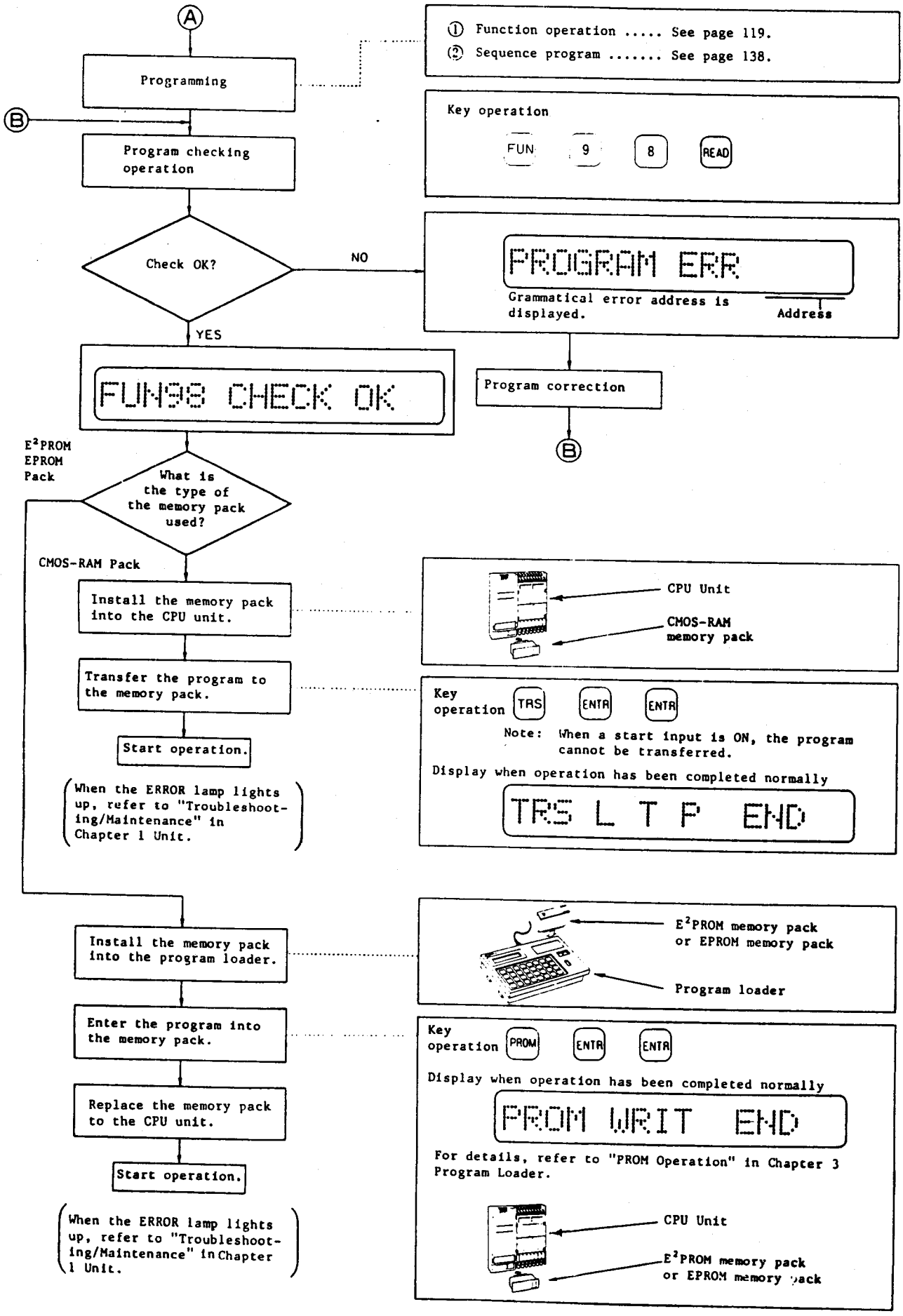
Register the program capacity.

Key operation



Note: Set the step according to the capacity of memory pack used. For details, see page 120.

Ⓐ


A
Programming
B
Program checking operation
Check OK?
NO
YES
FUN98 CHECK OK
E²PROM EPROM Pack
What is the type of the memory pack used?
CMOS-RAM Pack
Install the memory pack into the CPU unit.
Transfer the program to the memory pack.
Start operation.
When the ERROR lamp lights up, refer to "Troubleshooting/Maintenance" in Chapter 1 Unit.
Install the memory pack into the program loader.
Enter the program into the memory pack.
Replace the memory pack to the CPU unit.
Start operation.
When the ERROR lamp lights up, refer to "Troubleshooting/Maintenance" in Chapter 1 Unit.
① Function operation ..... See page 119.
② Sequence program ..... See page 138.
Key operation
FUN 9 8 READ
PROGRAM ERR
Grammatical error address is displayed.
Address
Program correction
B
CPU Unit
CMOS-RAM memory pack
Key operation TRS ENTR ENTR
Note: When a start input is ON, the program cannot be transferred.
Display when operation has been completed normally
TRS LTP END
E²PROM memory pack or EPROM memory pack
Program loader
Key operation PROM ENTR ENTR
Display when operation has been completed normally
PROM WRIT END
For details, refer to "PROM Operation" in Chapter 3 Program Loader.
CPU Unit
E²PROM memory pack or EPROM memory pack

PROGRAMMING KEY OPERATION

Clearing User Memory

To clear the entire program area.

DELT END ENTR

Setting or Reading Out Addresses

Addresses can be set or read out either during operation or not.

ADRS X X X → ↑ or ↓

Address No. — Read out in sequence

Entering Programs

After programs have been entered, they can be changed by superposing new programs.

1. END, MCS, MCR, JMP or JEND Instruction

INS ENTR

2. LOD, AND or OR Instruction

INS NOT □ X X X ENTR

- I/O or internal relay No.
- TIM, CNT or SFR
- Needed when inverting input

3. OUT Instruction

OUT X X X ENTR

I/O or internal relay No.

4. SOT Instruction

SOT X X ENTR

Single output No.

5. SET or RST Instruction

INS SFR X X X ENTR

- Output or internal relay No
- Needed for shift register

6. SFR Instruction

SFR NOT X X X ENTR

- Initial No. of shift register
- Needed for reverse shifting

X X X ENTR

No. of bits

7. TIM Instruction

TIM X X ENTR

Timer No.

X X X X ENTR

Preset value

NOTE: X denotes a numeric key. INS denotes an instruction key.

8. CNT Instruction

CNT X X ENTR

Counter No.

X X X X ENTR

Preset value

Changing Timer/Counter Preset Values during Operation

Timer or counter preset values can be changed during operation irrespective of the type of memory pack.

1. Read out the timer or counter number.

TRS □ X X READ

- No.
- TIM or CNT

2. Enter a new preset value.

X X X X ENTR

New preset value

Preset values stored in the memory pack are not changed by the above procedures 1 and 2.

> After changing a preset value, the new preset value can be cleared and the old value can be restored.
>
> FUN 9 5 READ → ENTR
>
> When this procedure is completed, all timer/counter preset values return to the original values.

3. Enter the new timer/counter preset values to the memory pack.

Stop operation.

Transfer the new preset values and program in the CPU unit to the loader.

FUN 9 4 READ · ENTR

Transfer the new preset values in the loader to the memory pack.

1) CMOS-RAM Memory Pack
Install the memory pack in the CPU unit.

TRS ENTR → ENTR

2) EPROM or E²PROM Memory Pack
Install the memory pack in the loader.

PROM ENTR → ENTR

Programs can be entered into a blank EPROM memory pack.

Deleting Programs

ADRS [X] [X] [X] · [↑] or [↓]

Initial address No. of deletion

DELT [X] [X] [X] ENTR

No. of programs to be deleted

After deletion, the subsequent programs are shifted up by the number of programs deleted.

NOTE When deleting two-address instructions (TIM, CNT, SFR, etc.), two addresses will be deleted at one time as one instruction.

Inserting Programs

ADRS [X] [X] [X] · [↑] or [↓]

Address No. to be inserted

Enter the program to be inserted. → INST

After insertion, the subsequent programs are shifted down.

Searching for Programs

A required program and its address can be searched for and displayed.

Program to be searched for → [↑] or [↓]

Example: To search for AND27

AND [2] [7] · [↑] or [↓]

Searching is started from the program next to the currently displayed program. When the required program is located, the program and its address are displayed.

Monitoring

1. Monitoring I/O and Internal Relays.

MON [X] [X] [X] → [↑] or [↓]

I/O or internal relay No.

Eight points are displayed at one time from the displayed address included, with ■ for ON or □ for OFF.

2. Monitoring Counted Values of Timers or Counters

MON [ ] [X] [X] · [↑] or [↓]

No.

TIM or CNT

Timers operate in the subtracting mode and counters in the adding mode. The counted value of the monitored timer or counter is displayed, with ■ when the preset value is reached or □ during counting.

3. Reading Out Contents of "ERR80"

MON CNT [↑] or [↓]

4. Monitoring Shift Registers

MON SFR [X] [X] [X] → [↑] or [↓]

Shift register No.

Eight bits from the displayed input number are displayed at one time, with ■ for ON or □ for OFF. Pressing the ↑ or ↓ key will display the next eight bits. Monitoring can be cancelled by pressing the CLR key. Monitored data is renewed every 100 msec.

5. Monitoring Scan Time

MON CNT 4 7 [↓] (See page 108.)

Transferring Programs between Loader and CPU Unit

1. Transfer from The Program Loader to The CPU Unit

TRS ENTR

When "TRS L T P GO?" is displayed, make sure the CPU unit is off and a CMOS-RAM memory pack is installed in the CPU unit. To continue, press the ENTR key. "TRS L T P" is displayed during execution. When completed, "TRS L T P END" is displayed.

2. Transfer from The CPU Unit to The Program Loader

TRS READ

When "TRS P T L GO?" is displayed, make sure this operation may be continued. To continue, press the ENTR key. "TRS P T L" is displayed during execution. When completed, "TRS P T L END" is displayed.

3. Verification between The CPU Unit and The Program Loader

TRS VERI

When "TRS L A P GO?" is displayed, make sure this operation may be continued. To continue, press the ENTR key. "TRS L A P" is displayed during execution. When completed, "TRS L A P END" is displayed.

Entering, Readout & Verification with PROM

1. Entering Programs into The Memory Pack

PROM ENTR

When "PROM WRIT GO?" is displayed, make sure this operation may be continued. To continue, press the ENTR key. "PROM WRIT" is displayed during execution. When completed, "PROM WRIT END" is displayed.

This operation can be canceled before completion by pressing the CLR key.

2. Reading out Programs from The Memory Pack to The Program Loader

PROM READ

When "PROM READ GO?" is displayed, make sure this operation may be continued. To continue, press the ENTR key. "PROM READ" is displayed during execution. When completed, "PROM READ END" is displayed.

3. Verifying Programs between The Memory Pack and The Program Loader

PROM VERI

When "PROM VERI GO?" is displayed, make sure this operation may be continued. To continue, press the ENTR key. "PROM VERI" is displayed during execution. When completed, "PROM VERI END" is displayed.

Function Operation

FUN X X X ↓

FUN No.

Program allocated to the FUN No. → ENTR

FUN (Function)

1. Set program conditions to the program loader by the FUN operation.
2. Program loader checkout and written program format error checkout can be performed.

- **Function list**

FUN No.	Functions	Enter	Page
FUN1	Program capacity readout and registration	Pack*	120
FUN2	PC error data readout and reset	—	121
FUN3	PC operating status readout	—	124
FUN4	Stop input No. readout and registration	Pack*	125
FUN5	Reset input No. readout and registration	Pack*	126
FUN6	Internal relay keeping designation, readout and registration	Pack*	127
FUN7	Counter keeping designation, readout and registration	Pack*	129
FUN8	Shift register keeping designation, readout and registration	Pack*	130
FUN30	Initial input No. registration for digital switch reading for external preset function	Pack*	131
FUN31	Initial output No. registration for digital switch selection for external preset function	Pack*	131
FUN32 to FUN34	Reserved Nos. (Unassigned)	—	—
FUN35	Selection and registration of "L" or "H" latch for external display function ("0": "L" latch)	Pack*	131
FUN60	Fiber link system device No. registration	Pack*	132
FUN61	Automatic start function registration (Automatic start when power is turned on)	Pack*	132
FUN93	Sequential monitor	—	133
FUN94	TIM/CNT preset value modified data readout	—	134
FUN95	TIM/CNT preset value modified data clearing	—	134
FUN96	Error status readout during cassette operation	—	135
FUN97	PC system version readout	—	—
FUN98	Program check	—	136
FUN99	Program loader hardware check	—	137

* Function operation should be programmed before a sequence program is entered.

Supplementary

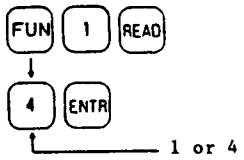
1. For function operation, be sure to read out all data before registration.
2. Function readout can be done continuously: registration processing, if any, can be carried out, then the data can be read out in succession.
3. For function registration, only items indicated with "Pack" in the list above are entered into the memory pack by the program transferring (entering) operation. Be sure to set function registration before transferring.

FUN (Function) Operation

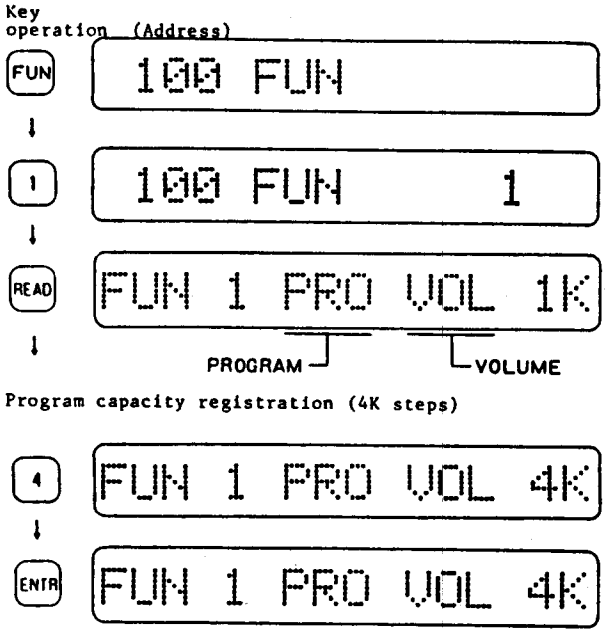
FUN1 Program Capacity Readout and Registration

1. Only when the 4K-step program loader PFA-1H404RE is used, the function operation is required.
   (1) When programming, register the capacity of program used first.
   (2) The program capacity should be registered, selecting either 1K or 4K steps according to the capacity of the program of the memory pack used.

Operation Sequence



- **Key operation and display**



Supplementary

1. When the memory is cleared, the program capacity of 1K steps is registered automatically.
2. With the 1K-step program loader (PFA-1H401RE), the program capacity can be read out by FUN1, but 4K-step writing is impossible. When the writing operation for 4K steps is performed, a buzzer alarm is generated signalling an error.
3. The registration of the program capacity can be modified at any time.

   Note: Setting must be completed before transferring a program to the memory pack.

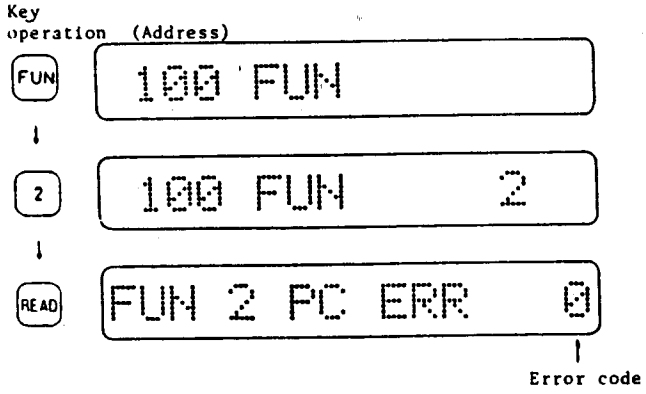
FUN2 PC Error Data Readout and Reset

1. This function reads out the status of errors which have occurred in the FA-1J.

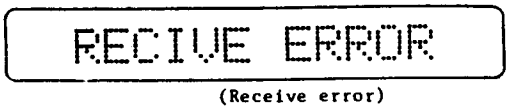
Operation Sequence

FUN 2 READ

- **Key operation and display**



Note 1: When the program loader is not connected to the CPU unit or no memory pack is installed in the CPU unit, the following error is displayed.

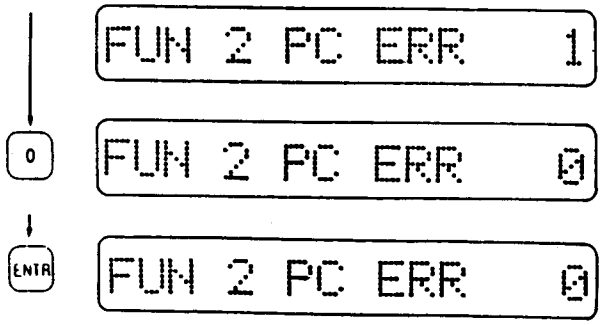


Error Data Code Resetting

Number "0" is entered into the error code display.

Key operation

FUN 2 READ



Note 1: Even when a number other than "0" is entered, the error data code can be reset in the same manner.

NOTICE

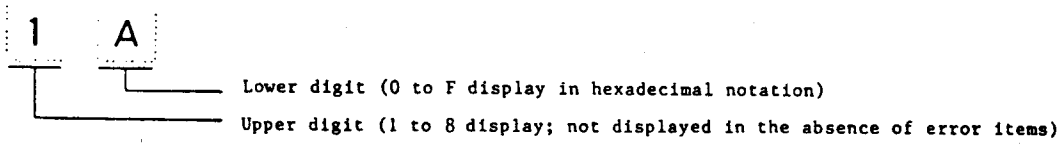
1. If the CPU unit is out of use for a long period of time, the super capacitor discharges, causing a wrong ERROR display. After turning power on, be sure to reset the error display.
2. Refer to Chapter 1 Unit - "Troubleshooting and Maintenance".

Supplementary 1

1. Error data code display and contents

   • The error code is displayed in one or two digits.

[Ex.]



2. For error codes, error conditions for four items in the lower digit and three items in the upper digit are displayed in a hexadecimal notation code.

(Lower digit error code display list)

Error Items / Lower Digit Error Code Display	Power Failure or Memory Pack Removal	WDT Error	Memory Pack Replacement	User Memory CRC Error
(No error) 0				
1	●			
2		●		
3	●	●		
4			●	
5	●		●	
6		●	●	
7	●	●	●	
8				●
9	●			●
A		●		●
B	●	●		●
C			●	●
D	●		●	●
E		●	●	●
F	●	●	●	●
ERROR lamp ON or OFF	OFF	OFF	OFF	ON

(Upper digit error code dispaly list)

Error Items / Upper Digit Error Code Display	TIM/CNT Preset Value CRC Error	User Memory Operational Code Error	Keeping Data Sum Check Error	FA-1J Program check
No display (No error)				
1	●			
2		●		
3	●	●		
4			●	
5	●		●	
6		●	●	
7	●	●	●	
8				●
ERROR lamp ON or OFF	OFF	ON	OFF	—

Note 1: Each error code display indicates that the error marked with • has taken place.
Two or more • marks indicate that a plurality of errors have occurred at the same time.

Note 2: Depending on the combination of errors in the upper digits, 9 to F may be displayed.

3. When the memory pack is removed and a memory pack with a different program is inserted again, Error Code 1 (Power failure or memory pack removal) and Error Code 4 (Memory pack replacement) are detected at the same time. Consequently Error Code 5 is displayed.
4. When the memory pack is removed and the same program memory pack is inserted again, Error Code 1 is displayed.
5. In the presence of two or more errors, it is indicated that all errors have occurred.
6. If the ERROR lamp on the CPU unit lights up, the unit stops operation. When the cause of the error is removed to restore operation, the ERROR lamp maintains its previous lighting condition; therefore, be sure to turn the ERROR lamp OFF from the loader according to the procedure "Error Data Code Resetting".
7. The display does not change even when the CPU unit's status changes after readout. Perform the FUN2 readout operation once again.

Supplementary 2

When "ERR80" occurs, the error contents can be read out by the following procedure.

- Key operation

- Display

Error code display

- Error items

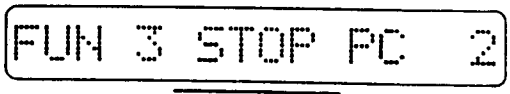
Display	Error Item
10000	Wrong FUN table setting. 1) I/O No. error of external digital switch setting (FUN30 & 31) 2) A number other than 0 is set by FUN32, 33 or 34. 3) Latch phase designation error for external display setting (FUN35) 4) HSC or HSL is set (FUN10 & 11) 5) Device No. error for personal computer communication (FUN60) 6) Automatic start designation error (FUN61) Note: 1) and 2) are checked when starting operation. 3) to 6) are checked even after stopping operation.
10001	I/O No. over error when executing external digital switch setting (FUN70 to FUN85)
Displays Address 0 to 4036	Instruction word near the displayed address is improper for computing operation. 1) Improper operator No. 2) Improper operand type 3) Improper operand value 4) More than 8 display instructions 5) Operator is absent but operand exists. 6) CNT47 instruction exists.

FUN3 PC Operating Status Readout

1. The base unit's operating status is read out.
   At the same time, the timer/counter preset value modification conditions are also displayed.

Operation Sequence

- **Display status**



RUN····· In operation
STOP··· Stopping

Status code
No display: T/C preset value is not modified.
2 : T/C preset value is modified.

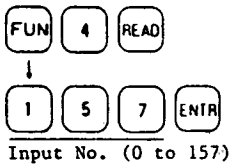
Supplementary

1. After reading out the data once, the display does not change even when the CPU unit's status changes. Perform the FUN3 readout operation once again.

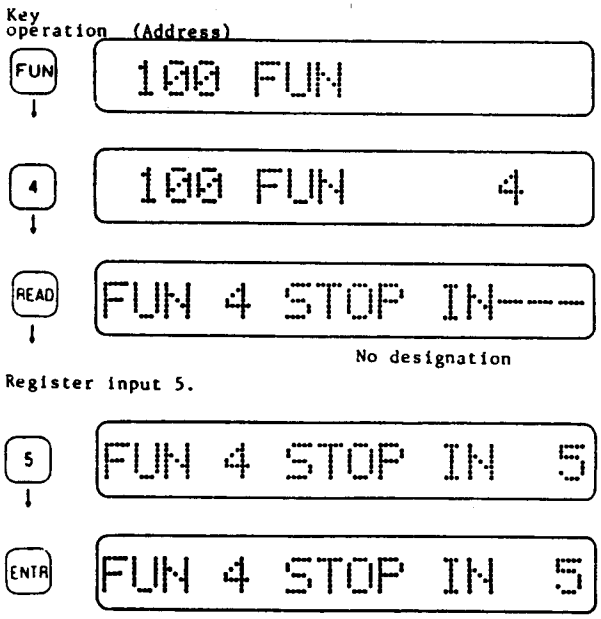
FUN4 Stop Input No. Readout and Registration

1. The FA-1J is not provided with a stop terminal; however, any input terminal can be designated as a stop terminal.
   When the designated stop terminal is turned ON, the FA-1J stops operation.

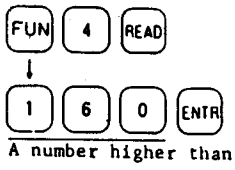
Operation Sequence



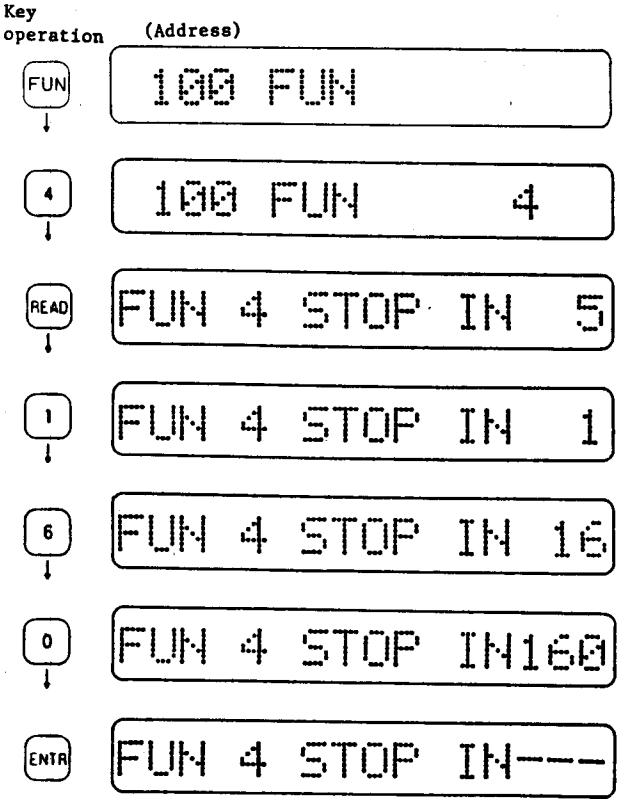
- **Key operation and display**



Clearing the Stop Input



- **Key operation and display**



Supplementary

1. Since the voltage level is detected for both the stop input and start input, operation is restarted if the stop input goes OFF while the start input is ON.
2. When both the start input and stop input are turned ON, the stop input has priority over the start input.
3. When stop input is designated, pulse inputs are accepted for both start and stop inputs.

Note 1: Setting must be completed before transferring a program to the memory pack.

Note 2: When a stop input is designated by FUN4, special internal relays 701 and 702 cannot be used to start or stop operation.

FUN5 Reset Input No. Readout and Registration

The FA-1J is not provided with a reset terminal; however, any input terminal can be designated as a reset terminal.
When the designated reset terminal is turned ON, all FA-1J conditions are reset.

Operation Sequence

FUN → 5 → READ
↓
1 → 5 → 7 → ENTR
Input No. (0 to 157)

- **Key operation and display**

Key operation	(Address)
FUN	100 FUN
5	100 FUN 5
READ	FUN 5 RESET ---
	No designation

Register input 12.

1	FUN 5 RESET 1
2	FUN 5 RESET 12
ENTR	FUN 5 RESET 12

Clearing the Reset Input

FUN → 5 → READ
↓
1 → 6 → 0 → ENTR
A number higher than input No.

- **Key operation and display**

Key operation	(Address)
FUN	100 FUN
5	100 FUN 5
READ	FUN 5 RESET 12
1	FUN 5 RESET 1
6	FUN 5 RESET 16
0	FUN 5 RESET 160
ENTR	FUN 5 RESET ---

Supplementary

1. Since the voltage level is detected for both reset and start inputs, operation is restarted if the reset input goes OFF while the start input is ON.
2. When both start and reset inputs are turned ON, the reset input has priority over the start input.

Note: Setting must be completed before transferring a program to the memory pack.

FUN6 Internal Relay Keeping Designation, Readout and Registration

1. The conditions of internal relays (IR400 to 697) are cleared during a power failure, but it is also possible to optionally designate the numbers of internal relays whose conditions are cleared (clear type relays) or maintained (keep type relays) when operation starts.
2. Internal relays from the designated number up to the last number (697) act as clear type internal relays.

[Ex.]

No. IR400 ------- 497 - 500 ----------No. 697

Keep type internal relays. | Clear type internal relays. (Designated number)

3. When all memories are cleared, "400" is set automatically; therefore, all internal relays are designated as clear type relays.

Operation Sequence

FUN 6 READ

↓

5 0 0 ENTR

Internal relay No. (400 to 697)

- **Key operation and display**

Key operation	(Address)
FUN	100 FUN
↓	
6	100 FUN 6
↓	
READ	FUN 6 IR 400
↓	

To designate clear type internal relays Nos. 500 to 697: (Nos. 400 to 497 are designated as keep type internal relays.)

5	FUN 6 IR 5
↓	
0	FUN 6 IR 50
↓	
0	FUN 6 IR 500
↓	
ENTR	FUN 6 IR 500

Supplementary

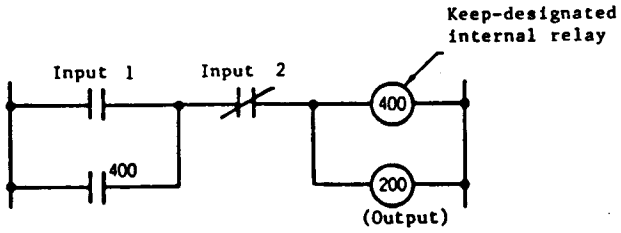
1. To designate all internal relays as keep type relays, set 700.
2. It is impossible to designate internal relay Nos. 400 to 697 intermittently.
3. The setting can be modified at any time.

Note: Setting must be completed before transferring a program to the memory pack.

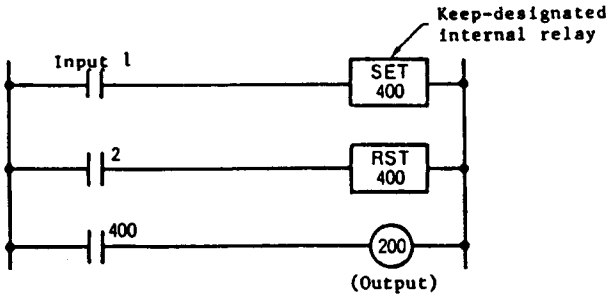
Sample Circuit Configuration

Keep type internal relays perform the same functions as clear type internal relays under normal service conditions. However, if power failure takes place after a keep type internal relay has been set in a self-holding circuit, the internal relay stores the status before power failure and operates when restart is initiated.

[Ex. 1]



[Ex. 2] When a keep type internal relay is self-maintained by the SET instruction, the status before power failure is also stored in the memory.



FUN7 Counter Keeping Designation, Readout & Registration

1. The counted values (adding type counter Nos. 0 to 44) are cleared during a power failure. It is also possible, however, to optionally designate counters whose counted values are cleared (clear type counter) or maintained (keep type counter) when operation starts.

2. Counters from the designated number up to the last number (No. 44) act as clear type counter.

   [Ex.]

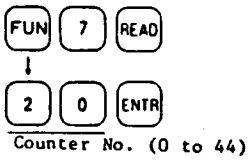
   Designated number

   Counter No. 0 ---------- 19 - 20 ---------- 44

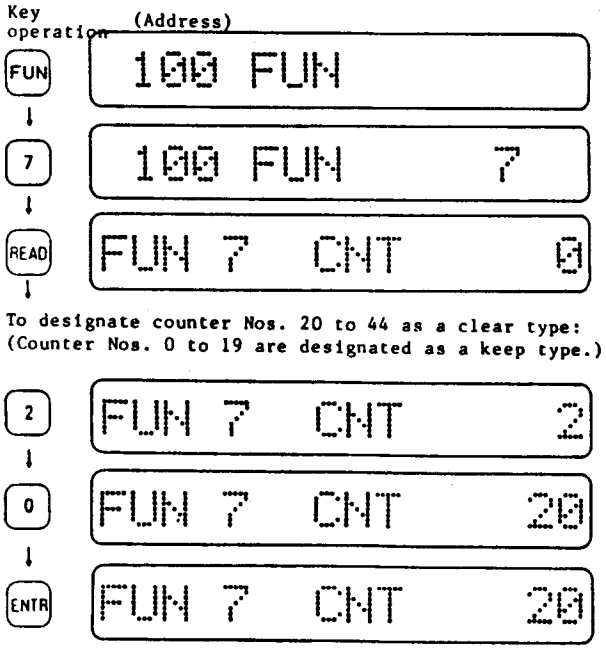
   Counted values are held at startup. | Counted values are cleared at startup.

3. When all memories are cleared, "0" is set automatically; therefore, all counters are designated as clear type counters.

Operation Sequence



- **Key operation and display**



Supplementary

1. To designate all counters (Nos. 0 to 44) as a keep type, set "45".
2. Reversible counters 45 and 46 are all keep type counters: however, counted values can also be programmed to be cleared when operation starts.
3. The preset values can be modified at any time.

Note: Setting must be completed before transferring a program to the memory pack.

FUN8 Shift Register Keeping Designation, Readout & Registration

1. The status of each bit (0 to 127) of the shift register is cleared during a power failure; however, it is also possible to optionally designate bits whose status is cleared (clear type) or maintained (keep type) when operation starts.

2. Shift registers from the designated bit No. up to the last bit No. (No. 127) act as clear type shift registers.

   [Ex.]

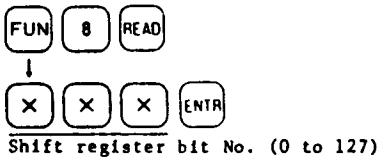
   Designated number

   Shift register bit No. 0 ---------- 39 - 40 ---------- 127

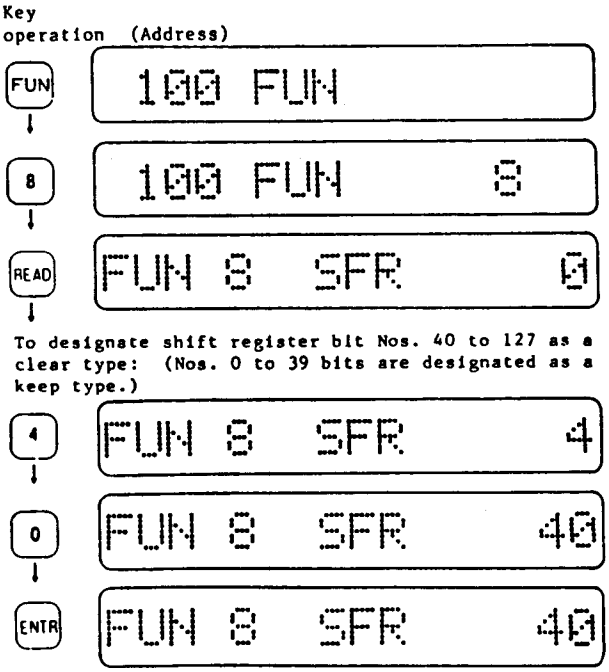
   Bit status is held at startup. | Bit status is cleared at startup.

3. When all memories are cleared, "0" is set automatically; therefore, all bits are designated as a clear type.

Operation Sequence



- **Key operation and display**



Supplementary

1. To designate all shift register bits (Nos. 0 to 127) as a keep type, set "128".
2. The preset values can be modified at any time.

Note: Setting must be completed before transferring a program to the memory pack.

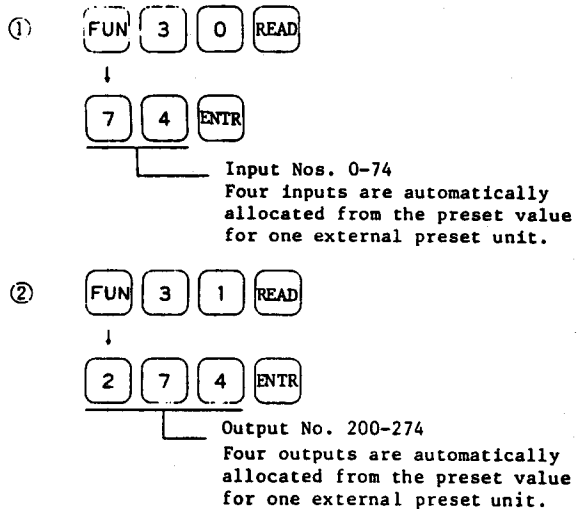
FUN30 Initial Number Registration of Digital Read Input When Using External Preset Function

FUN31 Initial Number Registration of Digitial Selection Output When Using External Preset Function

FUN30 and 31 are used in combination when using external preset function for setting timer/counter, preset values or computing values via external digital switches.

- FUN30: Sets the initial number of the input terminal to which a digital switch is connected.
- FUN31: Sets the initial number of the output terminal to which a digital switch is connected.

Operation Sequence



Supplementary

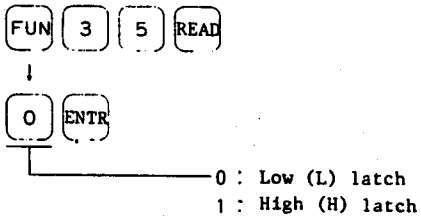
For details about the external setting function, see the section "Basic Instruction Word".

Note: Setting must be completed before transferring a program to the memory pack.

FUN 35 "L" or "H" Latch Selection Registration When Using External Display Function

FUN35 sets the latch condition of external digital display when using the external display function.

Operation Sequence



Supplementary

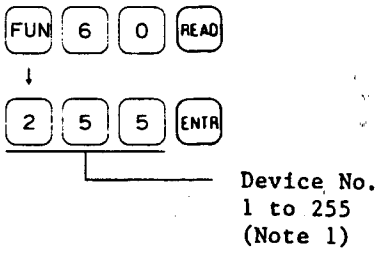
For details about the external display function, see the section "Basic Instruction Word".

Note: Setting must be completed before transferring a program to the memory pack.

FUN60 Fiber Link Communication Device Number Registration

FUN60 allocates a device number 1 to 255 to each CPU memory pack in sequence when constructing a fiber link system.

Operating Sequence



Supplementary

- Only the CPUs with the device numbers called from the center (personal computer) side via a device number designation command can be communicated.
- If FUN60 is set to 255 or more, an error (ERR80) will result when starting operation.
- Same numbers can not be designated to two or more CPUs connected in a fiber link system.
- When the user program is cleared, FUN60 is set to 0.

Note 1:
The program allows for setting 1 to 255, but a maximum of 32 CPUs can be connected.

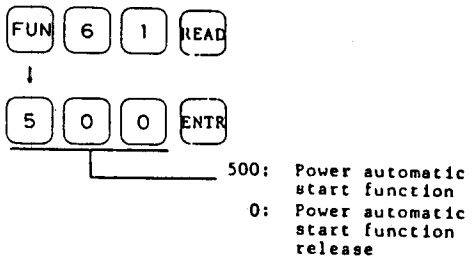
Note 2:
Setting must be completed before transferring a program to the memory pack.

FUN61 Automatic Start Function Registration [Automatic Start via Power Supply]

In the FA-1J unit, input terminal No. 0 can be used as a start terminal, but automatic start/stop via power supply is also possible using FUN61.

Operation Sequence

When FUN61 is set to 500, start function of input No. 0 is released and it can be used as normal input.



Supplementary

- "0" is set upon program all-clear operation.
- If a numeral other than 500 and 0 is set, it will be written in the program loader and memory pack, but the ERROR lamp will light and operation will not start upon turning on power of the FA-1J.

Note: Setting must be completed before transferring a program to the memory pack.

FUN93 Sequential Monitor

1. Monitoring functions include the 8-point simultaneous monitor function using the MON key and the sequential monitor using FUN93. The 8-point simultaneous monitor function performs monitoring for statuses at 8 points of I/Os, internal relays or shift registers simultaneously or one timer or counter status. The sequential monitor performs monitoring for the status of an I/O, internal relay, shift register, timer or counter instruction written at each address sequentially.
2. The sequential monitoring can be performed at each address containing a LOD, AND, OR, OUT, SET, RST, TIM or CNT instruction.
3. Monitor Display
   - ●I/O, IR or SFR
     - ■: ON
     - □: OFF

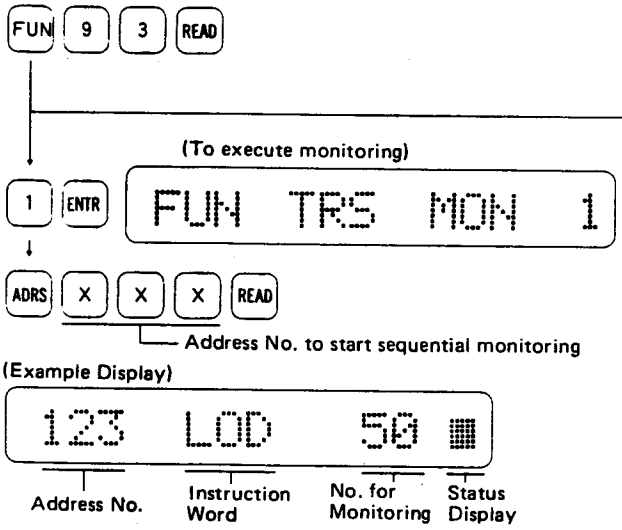
     No display: Communication or sequential monitoring is impossible at the address (instruction word).
   - ●Timer or Counter
     - ■: Time-up or count-up
     - □: During counting or in halt

     No display: Communication or sequential monitoring is impossible at the address (instruction word).

   Where a NOT instruction is included, the display is reversed.
   - □: ON (time-up or count-up)
   - ■: OFF (during counting or in halt)

Operation Sequence

●Key Operation

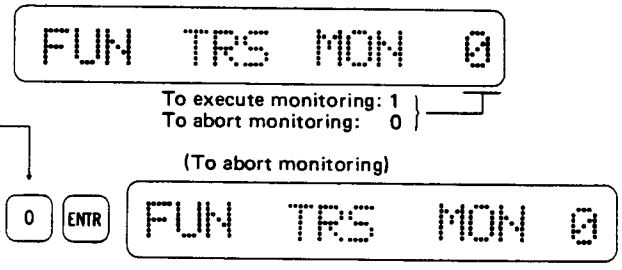


The above example of display indicates that Input 50 of the LOD instruction written at Address 123 is ON.

The preceding or subsequent address can be monitored simply by pressing the ↑ or ↓ key.

Unless the sequential monitoring is canceled, reading an address will execute monitoring the address continuously.

●Display



Supplementary

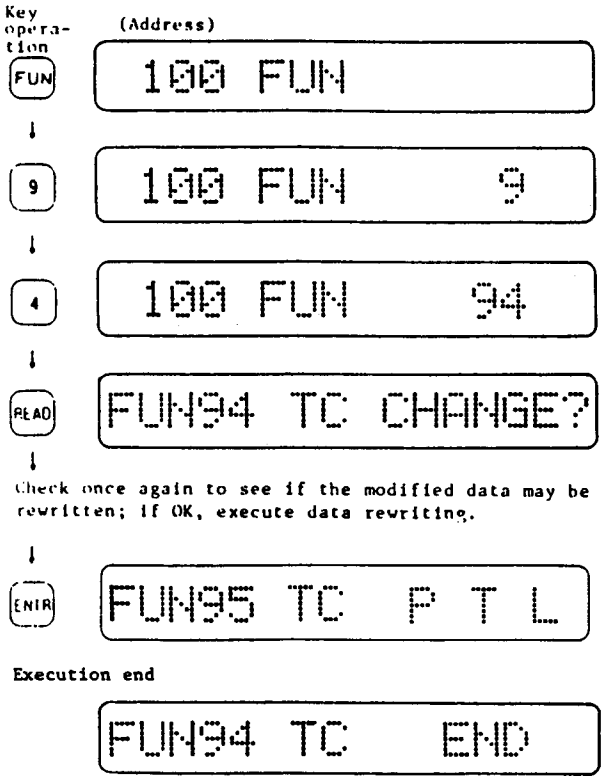
1. With FUN93 set to 1, each instruction key can be entered.
2. With FUN93 set to 1, however, if the program loader is powered by an AC adapter without connecting the loader to the CPU module, response to strokes on instruction keys will slow down. Set FUN93 to 0 before pressing instruction keys.

FUN94 TIM/CNT Preset Value Modified Data Readout

1. When preset values of timer (TIM), or counter (CNT) are modified during operation, it is possible to rewrite the preset values of a program within the program loader to its new preset values.

Operation Sequence

- **Key operation and display**



Supplementary

1. Prior to execution, ensure that the program in execution coincides with the program within the program loader.

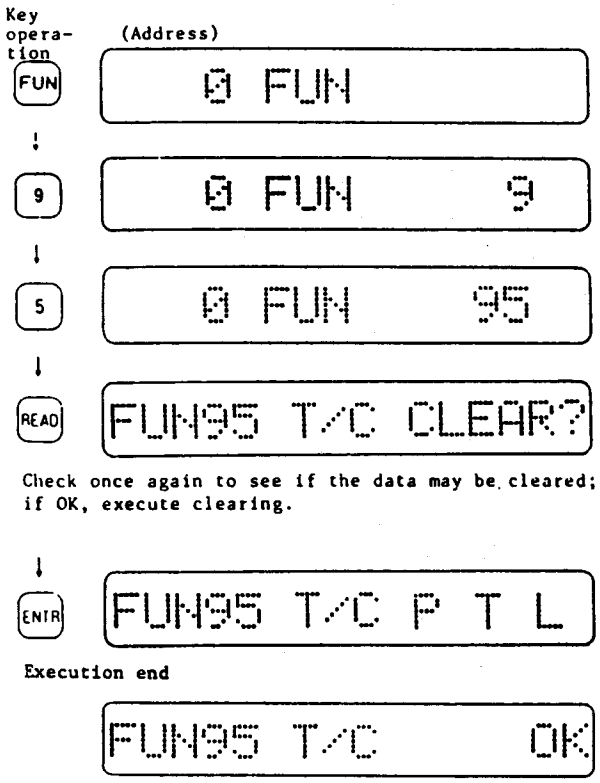
2. For the modification procedure of preset values during operation, refer to "Changing Timer and Counter Preset Values during Operation" on page 144.

FUN95 TIM/CNT Preset Value Modified Data Readout

1. Modification of timer and counter preset values can be cleared to restore the preset values before modification.

Operation Sequence

- **Key operation and display**



Supplementary

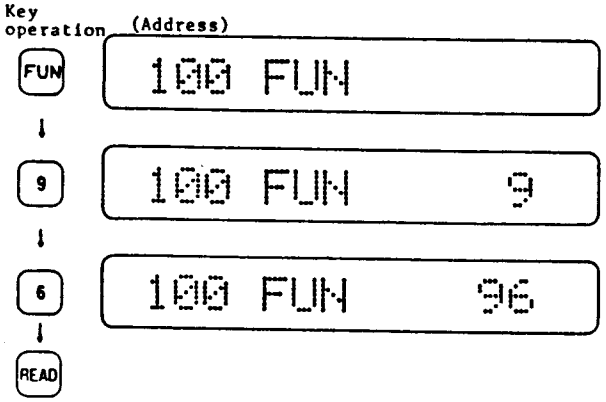
1. When FUN95 is executed, the preset value programmed in the memory pack is set.

FUN96 Error Status Readout during Cassette Operation

1. When an error is displayed on the program loader's display during cassette operation, error details can be checked.

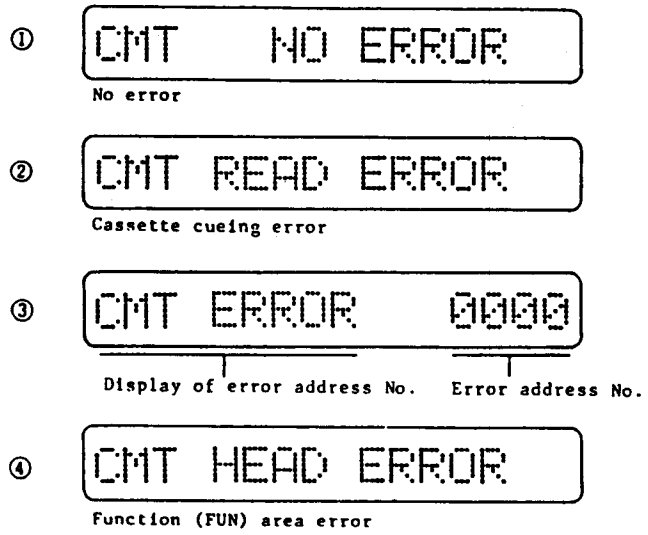
Operation Sequence

- **Key operation and display**



Four types of errors are on the display depending on their contents.

- **Error display**



Supplementary

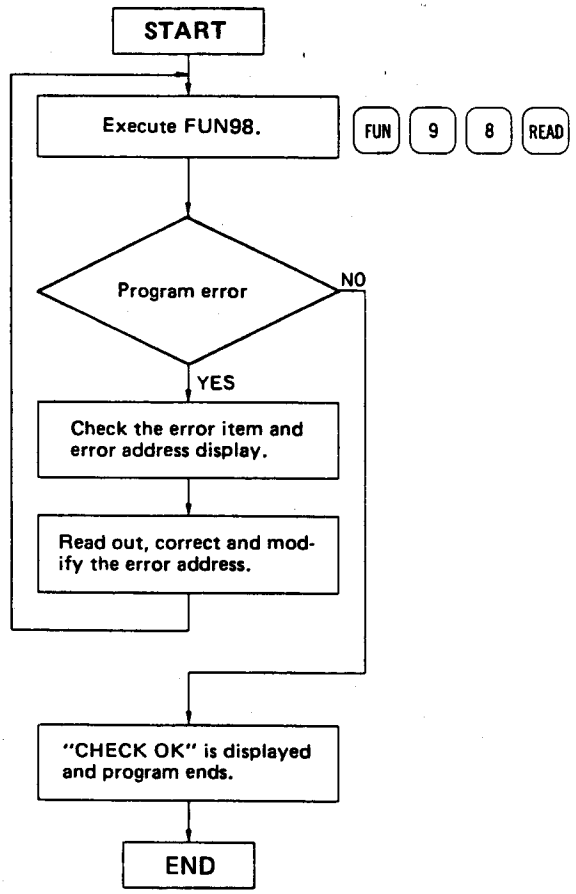
1. Once FUN96 is executed, error memory is cleared automatically.

FUN98 Program Check

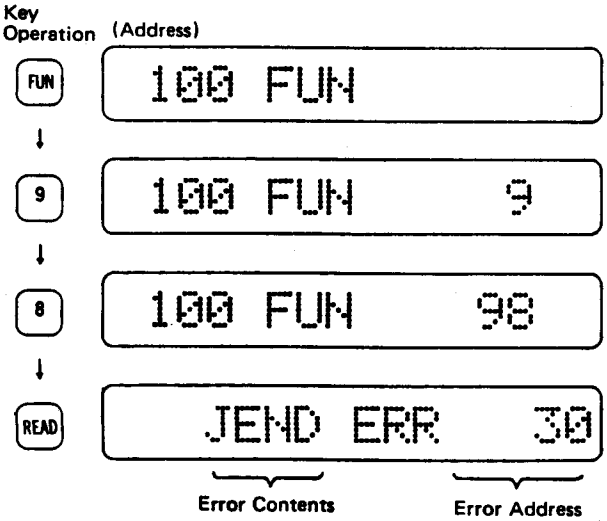
User programs can be checked. Programs are checked for every step: if an error is found, the error item and its address are displayed. Programs should be modified or corrected for every error displayed, and FUN98 execution should be repeated until a "CHECK OK" is displayed.

Operation Sequence

Upon completion of program input, check the program using the following steps.



● Key Operation and Display



Check Display

● The check display comes in seven types as follows depending on the contents.

① FUN98 NO PROGRAM

No user program has been inputted.

② END ERROR

No "END" has been inputted into the program.

③ MCR ERR 153

Only MCS or MCR has been inputted.

④ JEND ERR 217

Only JMP or JEND has been inputted.

⑤ PROGRAM ERR 10

● Only either of the two-address instruction is inputted.
● User program is damaged.

⑥ SIZE ERR SYS

Program capacity data is damaged.

⑦ FUN98 CHECK OK

Program check end message

Supplementary

In the presence of more than one error within one program, the error at the smallest address is displayed.

FUN99 Program Loader Hardware Check

1. The program loader display unit and internal memory function can be checked.
2. During the display test, all bits from 0 to 9 are displayed: check the displayed characters.
3. For internal memory function checkout, the entire internal RAM's readout and writing are checked. (Checking is carried out for every 0.5K byte, displaying ▩ .)

• Key operation and display

FUN 9 9 READ

If all functions are normal, the following is displayed, thus completing the processing.

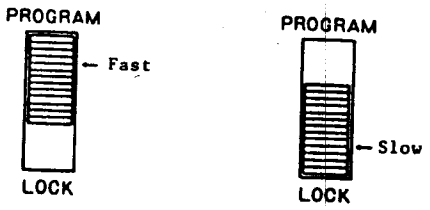
```
RAM TEST OK
```

When an error occurs during internal RAM checking, the display is as follows.

```
MEMORY ERROR A
```

Supplementary

1. The program/lock selector switch can be used to change checking speeds.



Program Basic Operating Procedures

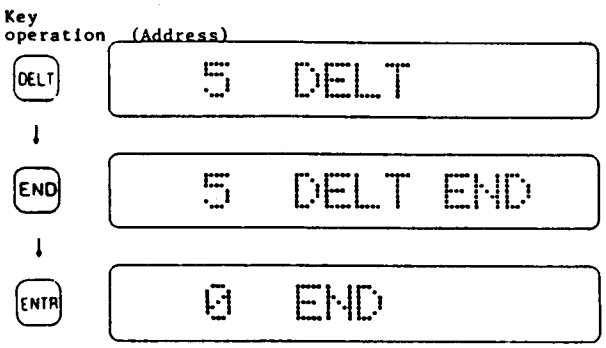
1. Clearing User Memory

1. The entire program memory within the program loader is cleared. Be sure to do this before starting programming.
2. After memory erasure, "END" instructions are written at each step.

Operation Sequence

DELT → END → ENTR

- **Key operation and display**



Supplementary

1. When the program/lock selector switch is set at "LOCK", execution is not possible.
2. All "FUN" settings are also cleared. Upon completion of clearing, the program capacity of the program loader is set at 1K steps.
3. The program in the memory pack is not cleared.

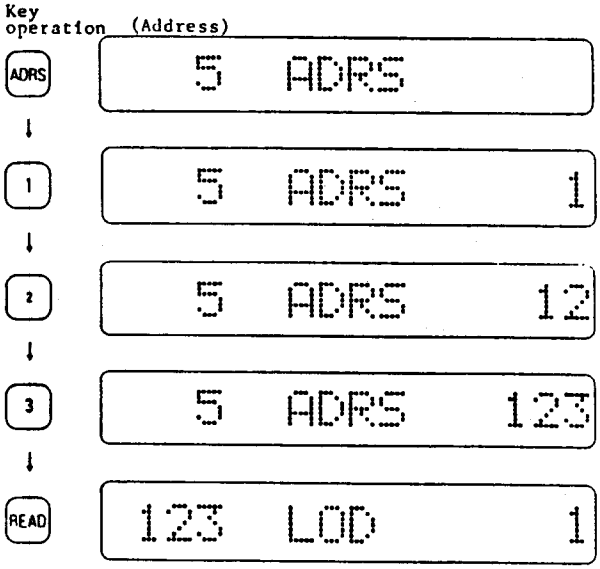
2. Setting Addresses

1. It is possible to set any address of the program within the program loader. When the designated address is larger than the maximum value (964 steps for 1K steps and 4,036 steps for 4K steps), the error buzzer alarm is given, thereby stopping execution: in this case, enter the proper address.

Operation Sequence

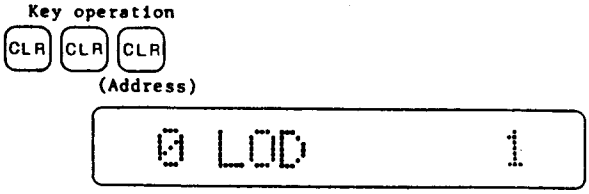
ADRS → ADRS NO → READ → (VERI)

- **Key operation and display (to set address 123)**



Supplementary

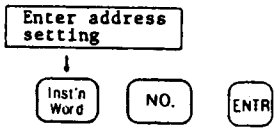
1. Key operation is possible whether the base unit is in operation or not.
2. When the CLR key is pressed continuously three times, the address is set at "0".



3. Entering Program Instructions

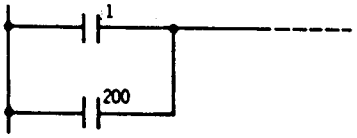
1. Enter a program instruction into the memory within the program loader.
2. When the ENTR key is pressed, the format and data are checked: if an error occurs, the buzzer sounds, and the program instruction is not entered.
3. Upon completion of program writing, the address is incremented by 1 and the program at that address is displayed.

Operation Sequence



- **Key operation and display**

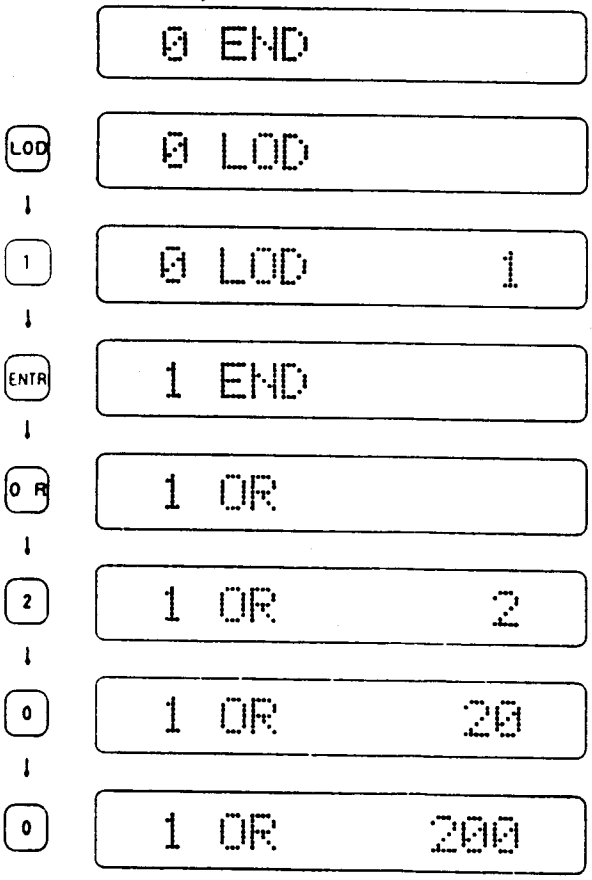
The operation procedure for this sample circuit is shown.



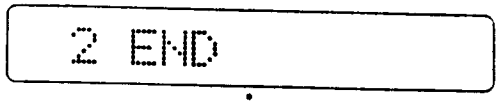
Key operation

ADRS 0 READ

(Address)

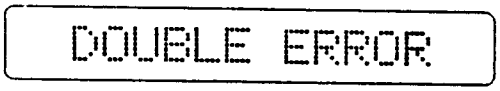


ENTR

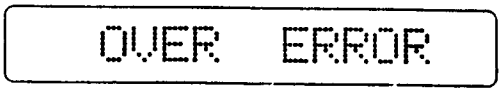


Supplementary

1. No writing operation is possible when the Program/Lock selector switch is at LOCK.
2. The OUT instruction cannot normally be used in double; however, since this may be required for programming with the FA-1J, an error buzzer sounds, but the program can be entered. (Use in double is such that the same output No. is used more than once.)
3. The same number cannot be used for both timer and counter instructions. When writing, a "DOUBLE ERROR" is displayed.



4. When programming instructions (TIM, CNT or SFR) requiring two addresses, the first-address instruction must be programmed first, otherwise the program instruction cannot be entered.
5. For a program capacity of 1K steps, the last address is step 964, where only the END instruction can be programmed. At address 963, a two-address instruction (TIM, CNT or SFR) cannot be programmed. When a wrong operation is carried out, the following message is displayed.



For a program capacity of 4K steps, the last address is step 4,036, and this is the same with 1K steps.

4. Reading Out Program Instructions

1. Programs within the program loader can be read out upward or downward in sequence.
2. By pushing the ⬇ or ⬆ key, the address is moved up or down sequentially in the direction of the arrow, and each program instruction is displayed.

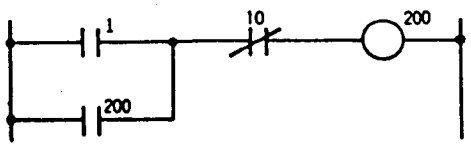
Operation Sequence

[READ] ..... This key reads out the values sequentially downwards.

[VERI] ..... This key reads out the values sequentially upwards.

- **Key operation and display**

The operation procedure for this circuit example is as follows.

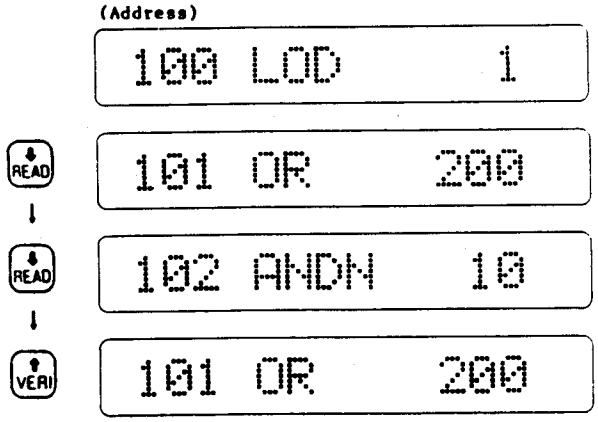


Address	Inst'n Word	Data
100	LOD	1
101	OR	200
102	AND N	10
103	OUT	200

Key operation
(To read out top address setting)

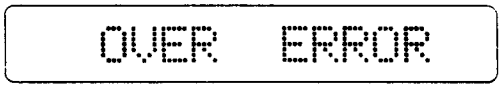
[ADRS] [1] [0] [0] [READ]

(Address)



Supplementary

1. When reading out the address next to the last address, the "OVER ERROR" message is displayed.



5. Deleting Program Instructions

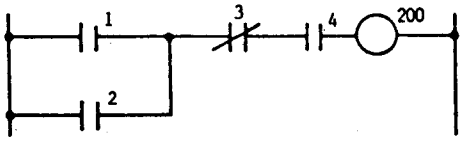
1. It is possible to delete a specified number of program instructions in the program loader starting from the address presently displayed.
2. Upon completion of deletion, the effective program is shifted up.

Operation Sequence

Read out the top address to be deleted.
↓
DELT → No. of instructions to be deleted → ENTR

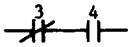
- **Key operation and display**

The operation procedure for this circuit example is as follows.



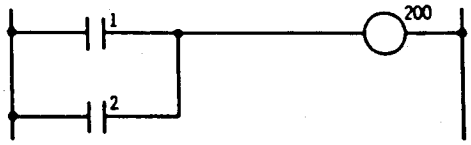
Address	Inst'n Word	Data
90	LOD	1
91	OR	2
92	AND N	3
93	AND	4
94	OUT	200

The following in this program is deleted:



To delete the above, delete the two instructions at addresses 92 and 93.

Program after deletion



Address	Inst'n Word	Data
90	LOD	1
91	OR	2
92	OUT	200

Key operation
(To set the top address 92 to be deleted)

ADRS → 9 → 2 → READ

(Address)

(Input the number of program instructions to be deleted, 2)

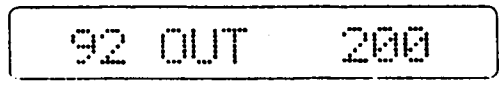
DELT

↓

2

↓

ENTR



Supplementary

1. No writing operation is possible when the Program/Lock selector switch is set at "LOCK".
2. When an instruction (TIM, CNT, SFR, FUN100 to 147, FUN200 to 247, FUN300, TIM·FUN, or CNT·FUN) requiring two addresses is included in the program to be deleted, both addresses are deleted as one program instruction; therefore, the number of specified program instructions does not coincide with that of deleted program addresses.

[Ex.]

The top address to be deleted (No. of addresses to be deleted: 1) →

Address	Inst'n Word	Data	
50	LOD	1	
51	TIM	5	Simultaneously deleted
52		50	
53	LOD	2	
54	AND	3	

↓

Address	Inst'n Word	Data
50	LOD	1
51	LOD	2
52	AND	3

3. When the deleting operation is carried out with the second address of a two-address instruction on the display, two addresses are deleted as one instruction.

The top address to be deleted (No. of addresses to be deleted: 1) →

Address	Inst'n Word	Data	
50	LOD	1	
51	TIM	5	Simultaneously deleted
52		50	
53	LOD	2	
54	AND	3	

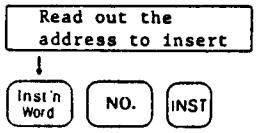
↓

Address	Inst'n Word	Data
50	LOD	1
51	LOD	2
52	AND	3

6. Inserting Program Instructions

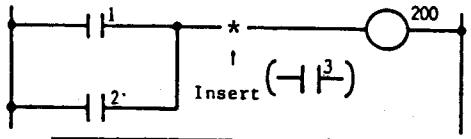
1. A program instruction can be inserted at any address.
2. After reading out the address to insert a program instruction, input the program instruction in the same format as with program writing, except pressing the INST key instead of the ENTR key. The existing program instructions from the designated address to the last address are shifted down by one step, and the entered program instruction is inserted.

Operation Sequence



• Key operation and display

The operation procedure for this circuit example is as follows.



Address	Inst'n Word	Data
10	LOD	1
11	OR	2
12	OUT	200

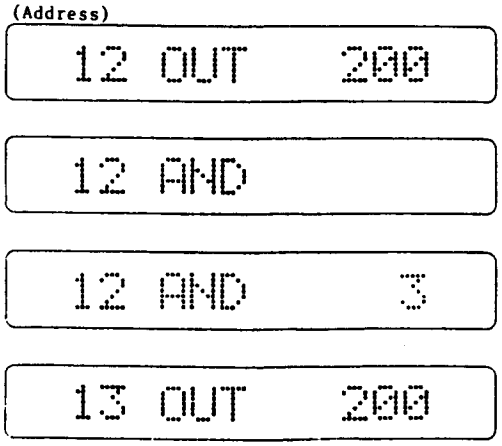
The following is inserted at the asterisked (*) position in this program: ⊣|3|⊢

For this purpose, insert an "AND3" between addresses 11 and 12.

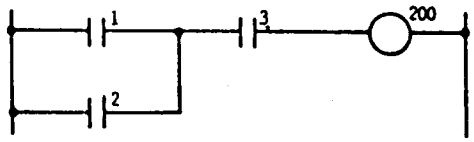
Key operation
(To set address 12 for insertion)

ADRS 1 2 READ

(Address)



Program after insertion



Address	Inst'n Word	Data
10	LOD	1
11	OR	2
12	AND	3
13	OUT	200

Supplementary

1. Program instructions cannot be inserted when the second address of a two-address instruction (TIM, CNT, etc.) is displayed.
2. Insertion is not possible at the second address of a two-address instruction. First insert an instruction word at the first address, then insert data at the second address.

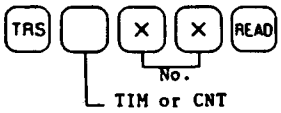
7. Changing Timer and Counter Preset Values during Operation

Preset values for timer and counter can be modified during operation regardless of the type of memory pack.

Operation Sequence

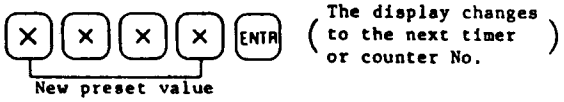
1) Read out the Timer (or Counter) No. to modify.

Key operation

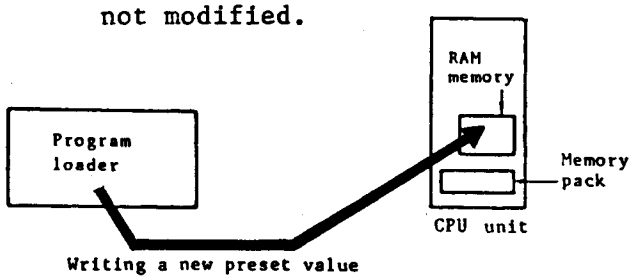


Display

2) Program a new preset value.



Note: Since a new preset value is entered into the FA-1J CPU unit's RAM memory by operations 1) and 2) above, preset values for the program in the memory pack are not modified.

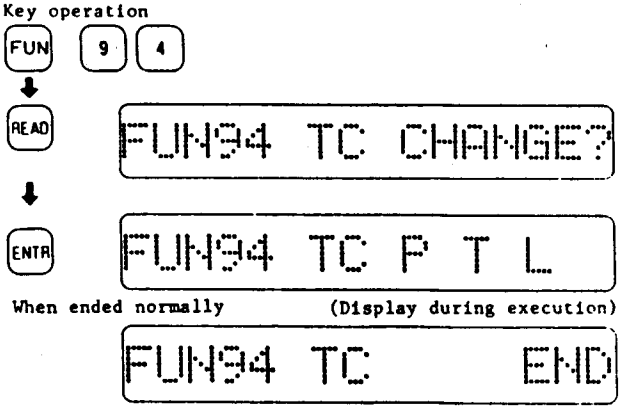


The RAM memory (new preset values for timer and counter) in the CPU unit is preserved for about one week (at 25°C) after power failure. However, when a CMOS-RAM pack is used, the memory is backed up by a battery in the memory pack.

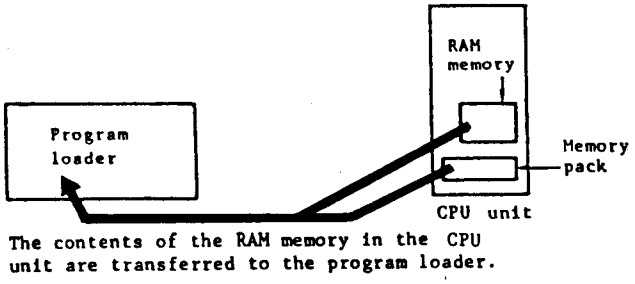
3) Enter new timer and counter preset values to be set or modified into the memory pack.

① Stop operation
② Transfer the new preset value and program presently in the RAM memory of the CPU unit into the program loader.

Key operation



- **Program and data movement**



③ Transfer the new preset value within the program loader to the memory pack.

- For CMOS-RAM
  Install the memory pack in the CPU unit.

  TRS ENTR – ENTR

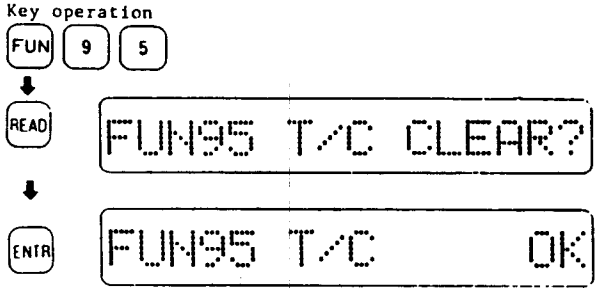
- For E^2PROM and EPROM*
  Install the memory pack in the loader.

  PROM ENTR – ENTR

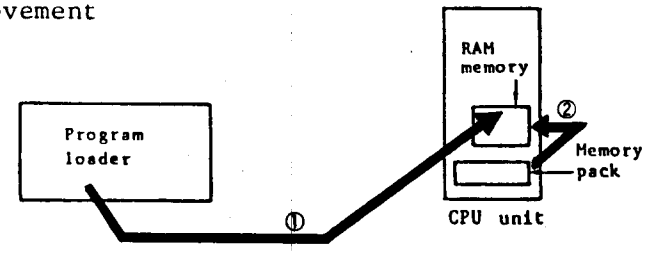
  * For EPROM, a program can be entered only into a new memory pack in which no program has been written.

Supplementary

1. To clear a modified preset value and restore the original preset value before modification:



Program and data movement



① Clear the CPU unit RAM memory.
② Enter the data (timer/counter preset values) within the memory pack into the RAM memory of the CPU unit.

In this operation, all timer and counter preset values are returned to their original condition before modification. Consequently, to restore specific timer/counter preset values, enter the original values according to the operation sequence in 1) and 2) above.

8. Operation by SET/RST Instructions

1. Input and output, etc. can be set (ON) or reset (OFF) directly from the loader only during operation, using the SET or RST instruction.
2. The following contents can be controlled.

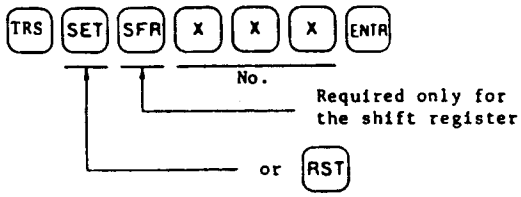
- Output : Nos. 200 to 357
- Internal relay: Nos. 400 to 697
- Special relay : Nos. 703 to 717
- Shift register: Nos. 0 to 127

① Both SET/RST instructions turn ON or OFF only when the ENTR key is depressed. When the next instruction is executed, both instructions perform the functions as per the sequence.

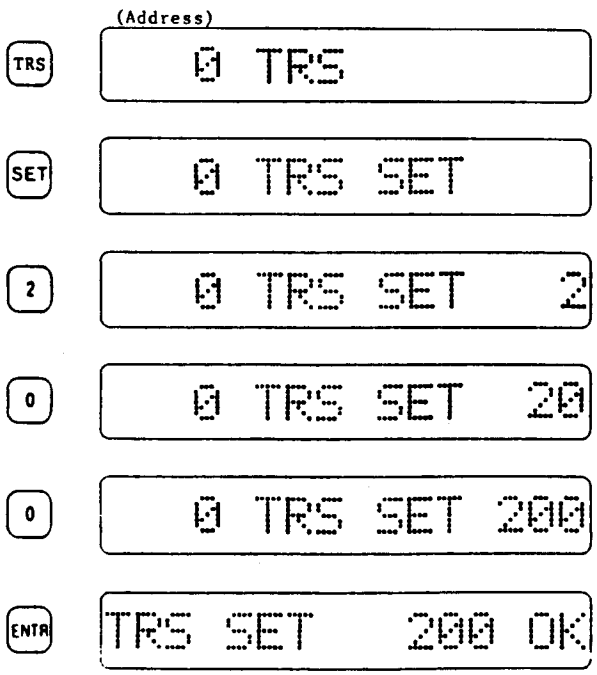
- Input : Nos. 0 to 157

② During one scan time, the input is set (ON) or reset (OFF).

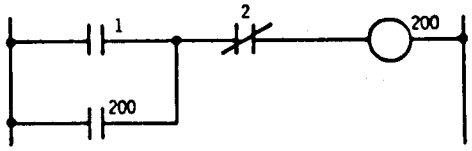
Operation Sequence



- Key operation and display
  (To set output No. 200)



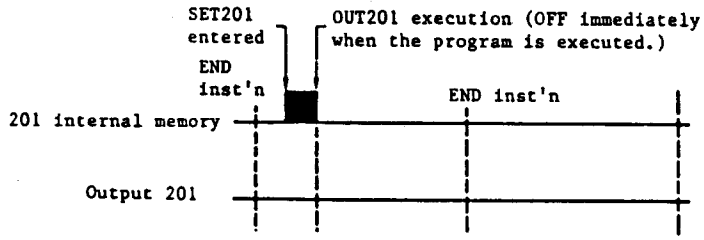
[Ex.] For the following circuit, input 1 is turned ON by the setting operation to actuate the self-holding circuit, and input 2 is turned OFF by the resetting operation to release the self-holding circuit.



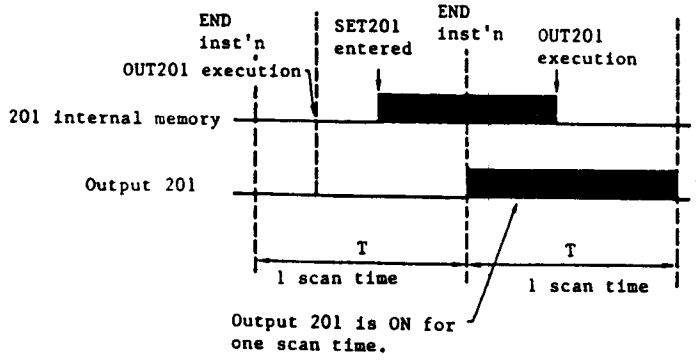
Supplementary

1. The time chart when the output in the following sample circuit is turned ON by the SET instruction:
   This time chart shows that with input 1 always OFF, there is a difference in operation between ① (before execution) and ② (after execution).

① When "SET201" operation is performed before OUT201 execution



② When "SET201" operation is performed after OUT201 execution



Note: 1. If internal memory 201 is ON during an END instruction execution, output 201 also goes ON, and if internal memory 201 is OFF, output 201 also goes OFF.

2. As described above, it should be noted that the output cannot be turned ON or OFF, depending on the output condition at the moment.

Retrieving Program Instructions

1. The address of the designated program instruction can be retrieved from the program in the program loader.
2. Retrieving can be performed by designating a required program instruction in the same manner as entering a program instruction, except pressing the ↓ or ↑ key instead of the ENTR key.
3. The designated program instruction is searched for in the direction of the arrow on the ↓ or ↑ key starting from the specified address, and when the designated instruction is located, its address is displayed.
4. If the designated instruction is not found, an error buzzer will sound, without changing the address display.

Operation Sequence

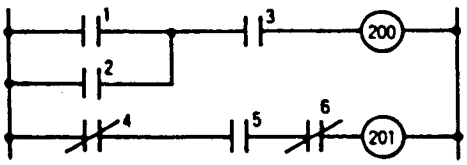
Read out the address to start retrieval.
↓
Program inst'n to be retrieved [↓] or [↑]

- **Sample designation for retrieving program instructions**

[LOD] [5] [↓]
[OUT] [2] [0] [0] [↓]
[TIM] [3] [↓]
[AND] [NOT] [TIM] [8] [↓]

Sample Retrieval

- **Relay diagram**



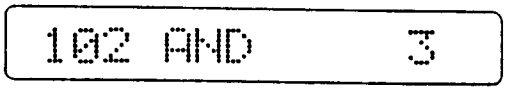
- **Program list**

Address	Inst'n Word	Data
⋮		
100	LOD	1
101	OR	2
102	AND	3
103	OUT	200
104	LOD N	4
105	AND	5
106	AND N	6
107	OUT	201

From the above circuit, the AND3 instruction is retrieved.

- **Key operation and display**

[ADRS] [0] [READ] Retrieval starts at Address 0.
[AND] [3]
[↓]

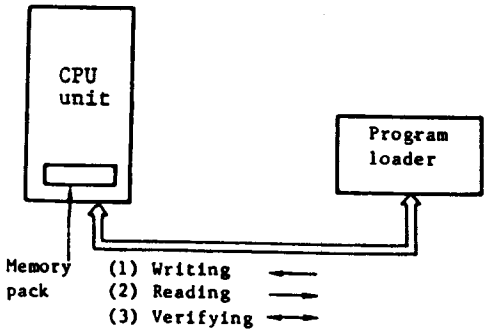


Supplementary

1. Even when the Program/Lock selector switch is set at LOCK, retrieval is possible.
2. Every program instruction is retrieved one at a time. Even the same program instructions cannot be retrieved continuously.

Transferring Program Instructions

1. Programs can be transferred between the memory of the program loader and the memory pack mounted in the CPU unit.
2. Transfer operation comes in three types:
   (1) Writing operation
   Writing programs from the program loader to the CMOS-RAM memory pack mounted in the CPU unit.
   (2) Reading operation
   Reading out programs from the memory pack mounted in the CPU unit to the program loader.
   (3) Verifying operation
   Verifying the program contents of the memory pack mounted in the CPU unit and the program contents within the program loader.



Supplementary

1. Writing operation is possible only when the CMOS-RAM memory pack is installed.
2. When the program loader is not connected to the CPU unit, a "Receive Error" message is displayed.

Display

RECIVE ERROR

3. When the Program/Lock selector switch of the program loader is set at LOCK, a buzzer signals that the operation is erroneous.
4. When a rewriting operation is carried out without changing the program in the program loader after the TIM/CNT preset values have been modified, the TIM/CNT preset values in the program loader are set.
5. When a writing operation is performed or the memory pack is replaced, the TIM/CNT preset values modified data is automatically cleared.

Relation between Transfer and Program Capacity

	Loader Program Capacity*		Memory Pack Program Capacity	Execution Result	Error Message
Write	1K	→	1K	A 1K-step program is entered into the FA-1J RAM pack.	———
	1K	→	4K	A 1K-step program is entered into the FA-1J RAM pack. The memory pack's program capacity becomes 1K steps.	———
	4K	→	1K	No writing is possible.	PC SIZE ERROR
	4K	→	4K	A 4K-step program is entered into the FA-1J RAM pack.	———
Readout	1K	←	1K	A 1K-step program is read into the program loader.	———
	1K	←	4K	No readout is possible.	SIZE ERR 4K
	4K	←	1K	A 1K-step program is read into the program loader. The program loader's program capacity becomes 1K steps.	———
	4K	←	4K	A 4K-step program is read into the program loader.	———

* When a 4K-step program loader is set to 1K steps, it has the same function as a 1K-step program loader.

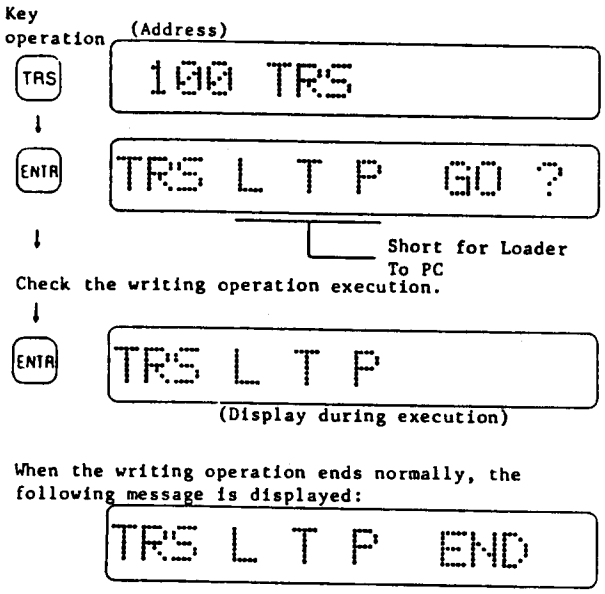
Note: The program capacity setting data (1K or 4K) preset in the program loader is also entered into the memory pack simultaneously with program transfer.

Writing Operation

Programs are entered from the program loader into the CMOS-RAM memory pack mounted in the CPU unit.

Operation Sequence

After checking that the RAM memory pack is installed and the FA-1J is not in operation, follow the steps below.

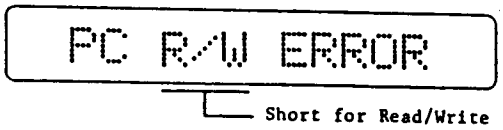


When the writing operation ends normally, the following message is displayed:

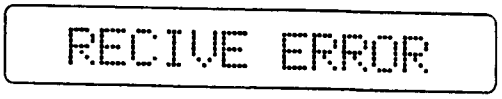
Error Display

1. When an EPROM or E^2PROM memory pack is installed in the CPU unit, no writing operation is possible, and the following error message is displayed.

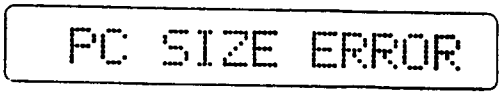
2. When a writing error occurs in the CPU unit, the following error message is displayed.



3. When a communication error occurs, the following error message is displayed.



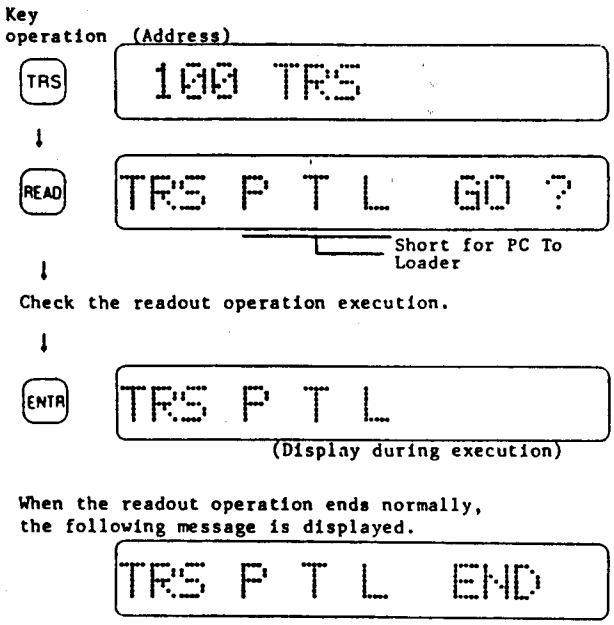
4. When a 4K-step program is written into a 1K-step memory pack, the following error message is displayed.



Readout Operation

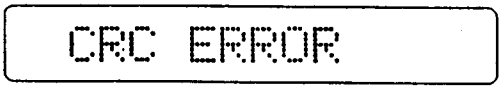
Programs are read out from the memory pack installed in the CPU unit to the program loader.

Operation Sequence

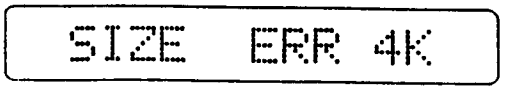


Error Display

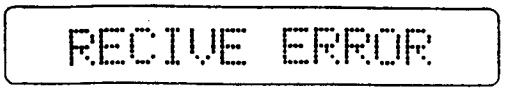
1. When program CRC checking finds an error, the following error message is displayed.



2. When the program capacity of program loader is set at 1K steps, (or a 1K-step program loader is used) and a 4K-step program is read, the following error message is displayed.



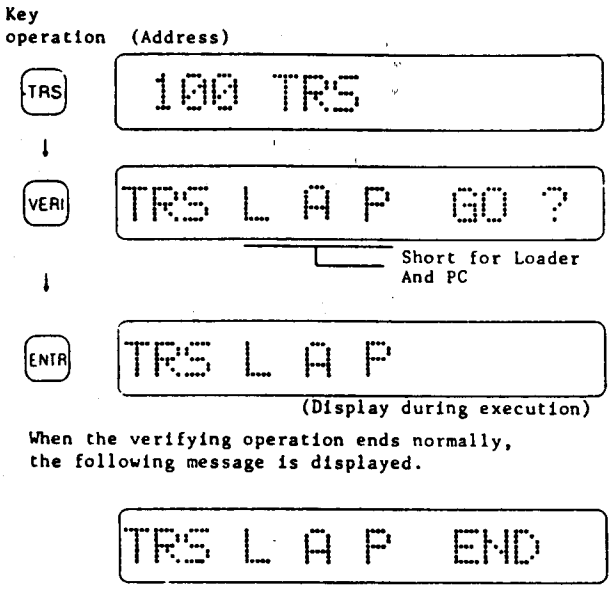
3. When a communication error occurs, the following error message is displayed.



Verifying Operation

Verification between the program of the memory pack installed in the CPU unit and the program within the program loader is performed.

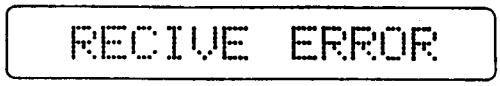
Operation Sequence



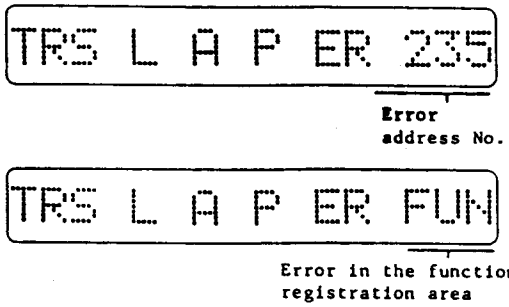
When the verifying operation ends normally, the following message is displayed.

Error Display

1. When a communication error occurs, the following error message is displayed.

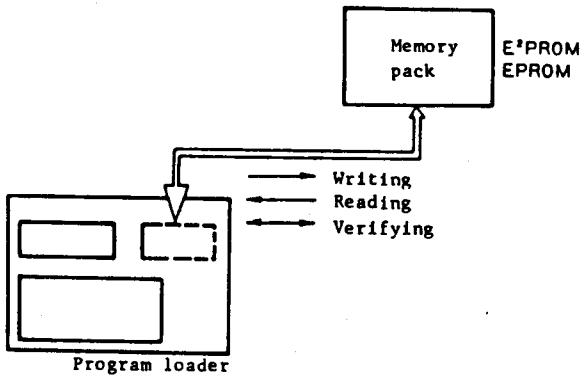


2. When a verification error occurs, the following error message is displayed.



PROM Writer Operation

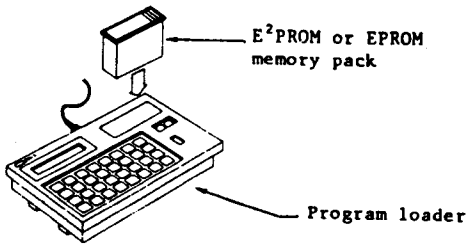
A program within the program loader can be written into an EPROM or E^2PROM, and a program in the memory pack can be read into the memory of the program loader. The contents of each program can be verified as well.



Note: Do not write, readout or verify a CMOS-RAM memory pack. The program may be possibly changed.

Supplementary

1. Prior to the PROM writer operation, install an E^2PROM or EPROM memory pack in the program loader.



2. When the Program/Lock selector switch is set at LOCK, an operational error occurs.
3. When stopping operation halfway, press the CLR key.
4. • Writing time
   E^2PROM 4K steps: Approx. 50 sec
   EPROM 4K steps: Approx. 6.5 min

   • Reading time
   E^2PROM 4K steps: Approx. 5 sec
   EPROM 4K steps: Approx. 25 sec

Relation between the PROM Writing Operation and the Program Capacity

	Loader Program Capacity*	Memory Pack Program Capacity	Execution Result	Error Message
Write	1K →	1K	A 1K-step program is entered into the memory pack.	——
	1K →	4K	A 1K-step program is entered into the memory pack. The memory pack's program capacity becomes 1K steps.	——
	4K →	1K	No writing is possible.	SIZE ERR 4K
	4K →	4K	A 4K-step program is entered into the memory pack.	——
Readout	1K ←	1K	A 1K-step program is read into the program loader.	——
	1K ←	4K	No readout is possible.	SIZE ERR 4K
	4K ←	1K	A 1K-step program is read into the program loader. The program loader's program capacity becomes 1K steps.	——
	4K ←	4K	A 4K-step program is read into the program loader.	——

* When a 4K-step program loader is set to 1K steps, it has the same function as a 1K-step program loader.

PROM Writing Operation

Programs within the program loader are written into an EPROM or E²PROM memory pack.

Operation Sequence

Key operation (Address)

PROM → 100 PROM

↓

ENTR → PROM WRIT GO ?

↓

Check the writing operation.

↓

ENTR → PROM WRIT

(Display during execution)

When the operation ends normally, the following message is displayed.

PROM WRIT END

Error Display

1. When an attempt is made to write a 4K-step program into a 1K-step memory pack, the following error message is displayed.

SIZE ERR 4K

2. When a writing data error occurs, the following error message is displayed.

PROM WRIT ER 315

Error address No.

3. When an EPROM has not yet been erased, the following error message is displayed.

PROM NOT ERASE

4. When the function setting area data within the program loader is abnormal, the following error message is displayed.

SIZE ERR SYS

5. When no memory pack is installed in the program loader, or a function setting area error occurs, the following error message is displayed.

PROM WRIT ER FUN

6. When the program capacity data of the memory pack is abnormal, the following error message is displayed.

SIZE ERR ***

PROM Readout Operation

The program can be read out of an EPROM or E²PROM memory pack mounted in the program loader.

Operation Sequence

key operation (Address)

PROM → 100 PROM

READ → PROM READ GO ?

Check the readout operation.

ENTR → PROM READ

(Display during execution)

When the readout operation ends normally, the following message is displayed.

PROM READ END

Supplementary

When the program capacity data is abnormal, the contents of the memory pack are not read. However, according to the following key operation, program reading becomes possible.

Key operation (Address)

PROM → 100 PROM

READ → PROM READ GO ?

FUN → PROM READF GO ?

ENTR → PROM READF

(Display during execution)

When ended:

PROM READF END

Error Display

1. When a memory pack program capacity error occurs, the following error message is displayed. This error occurs when attempting to read a program designated at 4K steps from a memory pack into a program loader designated at 1K steps.

SIZE ERR 4K

2. When an error occurs during writing a program into the memory of a program loader after reading out, the following error message is displayed.

PROM READ ER 315

Error address No.

3. When the read program CRC data is abnormal, the following error message is displayed. In this case, however, the program is read into the program loader.

CRC ERROR

4. When the memory pack is not mounted in the program loader, or when the memory pack's program capacity data is abnormal, the following error message is displayed.

SIZE ERR ***

PROM Verifying Operation

Verification between the program within the program loader and the program in the memory pack mounted in the program loader can be performed.

Operation Sequence

Key operation (Address)

PROM → 100 PROM

↓

VERI → PROM VERI GO ?

↓

ENTR → PROM VERI

(Display during execution)

When ended normally, the following message is displayed.

PROM VERI END

Error Display

1. When the program loader's program capacity is different from the memory pack's program capacity, the following error message is displayed.

SIZE ERR 4K

2. When a verification error occurs, the following error message is displayed.

PROM VERI ER 315

Error address No.

3. When a verification error occurs in the function registration area or when a memory pack is not mounted in the program loader, the following error message is displayed.

PROM VERI ER FUN

Audio Cassette Operation

Programs within the program loader can be recorded (written), played back (read out) and verified, using a commercially available audio cassette tape recorder.

Supplementary

1. When the Program/Lock selector switch is set at LOCK, cassette operation is not effected.
2. When stopping operation midway, press the CLR key.
3. Use the optional cassette cable (PL-C1) to connect the program loader to the tape recorder.

Relationship between Cassette Operation and Program Capacity

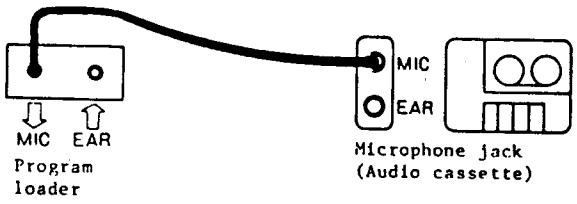
	Cassette Program Capacity Data	Loader Program Capacity*	Execution Result	Error Message
Readout	1K →	1K	A 1K-step program is read into the loader.	——
	1K →	4K	A 1K-step program is read into the loader. The loader's program capacity becomes 1K steps.	——
	4K →	1K	No reading is possible.	SIZE ERR 4K
	4K →	4K	A 4K-step program is read into the loader.	——

* When a 4K-step program loader is set to 1K steps, it has the same function as a 1K-step program loader.

Cassette Recording Operation

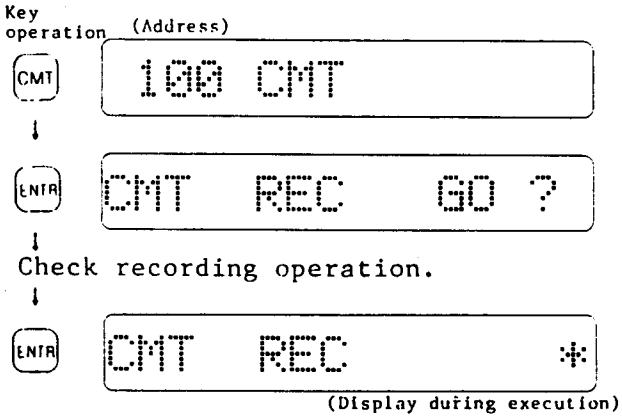
The program within the program loader is recorded onto a cassette tape.

Cable Connection



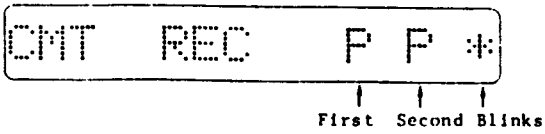
Operation Sequence

After checking that the cassette tape has been rewound completely, set the tape recorder to the REC mode and start the tape running.

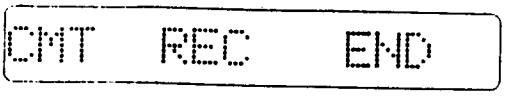


- Immediately after the ENTR key is pressed, * is displayed for approx. 14 seconds. During this period, the cueing mark is recorded. After that, * starts to blink, thus starting program recording.

- Recording is performed three times: if the recording is normal, a "P" is displayed at the end of each recording, or if it is abnormal, an "E" is displayed at the end of each recording.



When recording is completed three times, the following message is displayed.



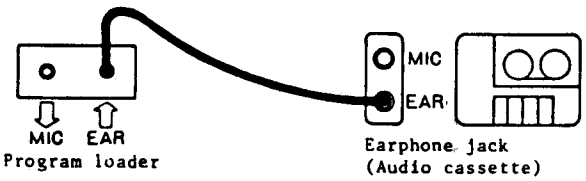
Recording Time Required

1K steps: Approx. 4 minutes 15 seconds
4K steps: Approx. 17 minutes

Cassette Playback Operation

The program recorded on a cassette tape is read out to the program loader memory.

Cable Connection



Operation Sequence

Key operation (Address)

CMT → 100 CMT

READ → CMT READ GO ?

Check the playback operation.

ENTR → CMT READ *

Simultaneously with pressing the ENTR key, set the cassette tape recorder to the PLAY mode.

- The playback operation ends when any one of the three recordings is read normally.

CMT READ END

- If an error occurs, an "E" is displayed, continuing the next reading.

CMT READ E E *

1st error, 2nd error

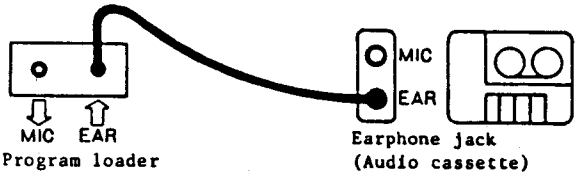
- When the program cannot be read, the following error message is displayed.

CMT READ ERROR

Cassette Verifying Operation

Verification between the program recorded on the cassette tape and the program of the program loader is performed.

Cable Connection



Operation Sequence

Key operation (Address)

CMT → 100 CMT

VERI → CMT VERI GO ?

ENTR → CMT VERI *

Simultaneously with pressing the ENTR key, set the cassette tape recorder to the PLAY mode.

- All three recordings are verified: if normal, a "P" is displayed, and if erroneous, an "E" is displayed.

CMT VERI P P *

First, Second, Blinks

When three verifications are completed, the following message is displayed.

CMT VERI END

- If at least one error occurs, the following error message is displayed at the end.

CMT VERI ERROR

Monitoring Operation

1. I/O performance and the counted values of timers, etc. can be readily monitored during operation, using the keyboard switches.

The following can be monitored:

(1) I/O performance status
(2) Timer counted values and performance status
(3) Counter counted values and performance status
(4) Internal relay performance status
(5) Shift register performance status

Others:

(6) Program remaining step display
(7) Scan time readout

2. The next data is updated and displayed, using the ↓ or ↑ key.

3. For the monitoring operation, always connect the CPU unit and program loader.

Supplementary

1. Monitored data is updated and displayed every 100msec.
2. To cancel the monitoring operation, press the CLR key.
3. Even when the program loader's Program/Lock selector switch is set at LOCK, monitoring can be performed.

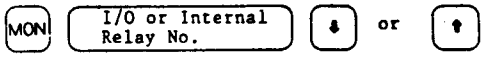
I/O and Internal Relay Monitoring Operation

1. The monitored status is displayed in units of 8 points, starting from the designated number.
2. The monitored state is displayed as follows.

■ ON display

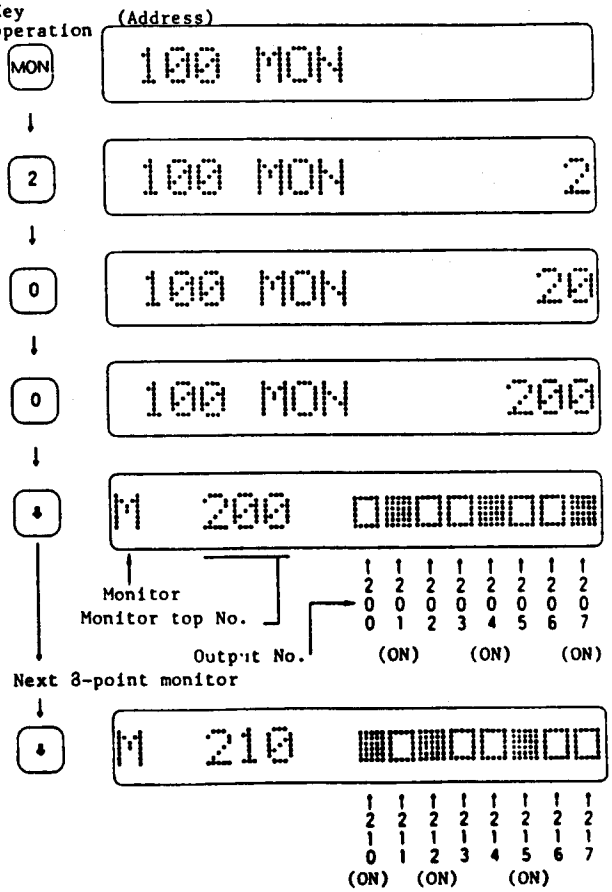
□ OFF display

Operation Sequence



- **Key operation and display**

[Ex.] To monitor Output No. 200:



Timer/Counter Monitoring Operation

1. The counted values are monitored in the subtracting mode for timers and in the adding mode for counters.
2. The monitor display includes the timer or counter number, counted value and ON/OFF-status.
3. For both counter and timer, the ON/OFF-status display is as follows.

   ■ ON (Time up or count up)
   □ OFF (Counting or stopping)

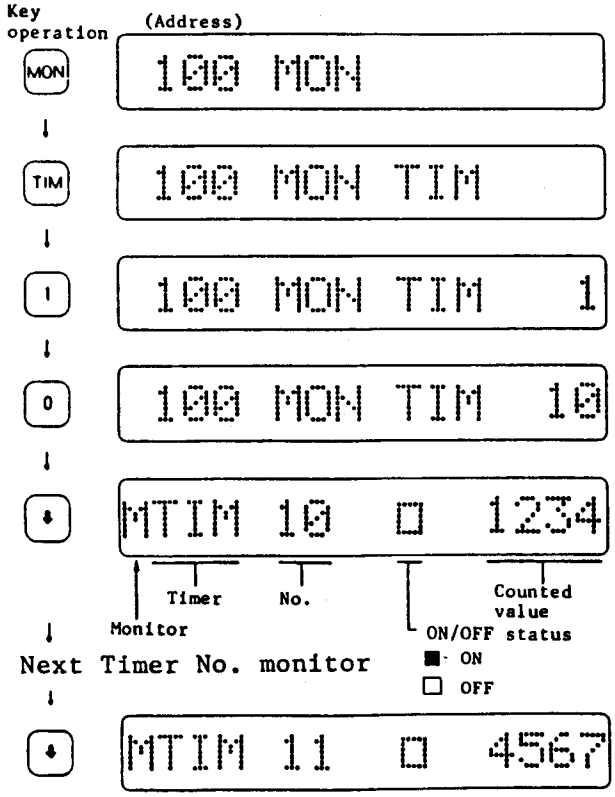
Operation Sequence

① MON → TIM → Timer No. → ↓ or ↑

② MON → CNT → Counter No. → ↓ or ↑

- **Key operation and display**

[Ex.] To monitor Timer No. 10:



Shift Register Monitoring Operation

1. The ON/OFF-status of each bit of the shift register is displayed in units of 8 points. The display is as follows.

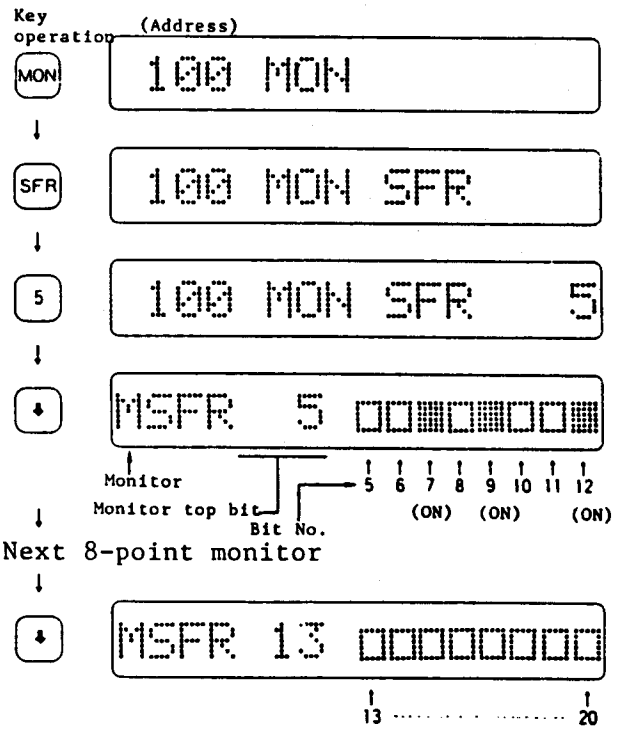
   ■ ON (1)
   □ OFF (0)

Operation Sequence

MON → SFR → Bit No. → ↑ or ↓

- **Key operation and display**

[Ex.] To monitor Bit No. 5 of the shift register:



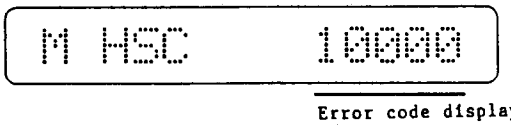
Reading Out ERR80 Contents

When "ERR80" occurs, the error contents can be read out by the following procedure.

Operation Sequence

Key operation

- Display



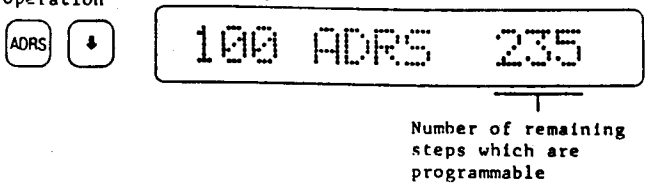
For details of error items, see page 123.

Program Remaining Step Display

The number of remaining steps within the program loader can be confirmed.

Operation Sequence

Key operation

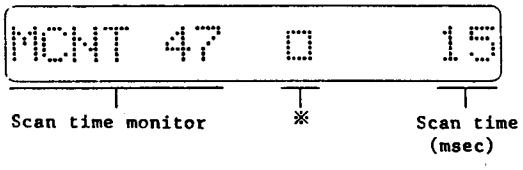


Reading Out Scan Time

The scan time of the program written in the FA-1J can be read out.

Operation Sequence

Key operation



※ No meaning

Reading Out Allocation Numbers

The following usable allocation numbers are read out and displayed.

1. Input No.
2. Output No.
3. Internal relay
4. Special relay
5. Timer
6. Counter
7. Shift register
8. Single output

Operation Sequence

MON ↓ or ↑

- **Key operation**

MON

↓ Input — M IN 0-157

↓ Output — M OUT 200-357

↓ Internal relay — M IR 400-697

↓ Special relay — M SP 700-717

↓ Timer — M TIM1 0- 63

↓ 10-msec Timer — M TIM2 64- 71

↓ External analog timer — M TIM3 72- 79

↓ Counter — M CNT 0- 47

↓ Shift register — M SFR 0-127

↓ Single output — M SOT 0- 95

Supplementary

1. Pressing the ↑ key moves the display in the reverse direction.
2. To cancel the readout, press the CLR key.

Reading Out Data Register (DR)

The contents of Data Registers DR0 to DR99 can be read out.

Data Register	Operand No.
DR0	800
DR1	801
DR2	802
DR99	899

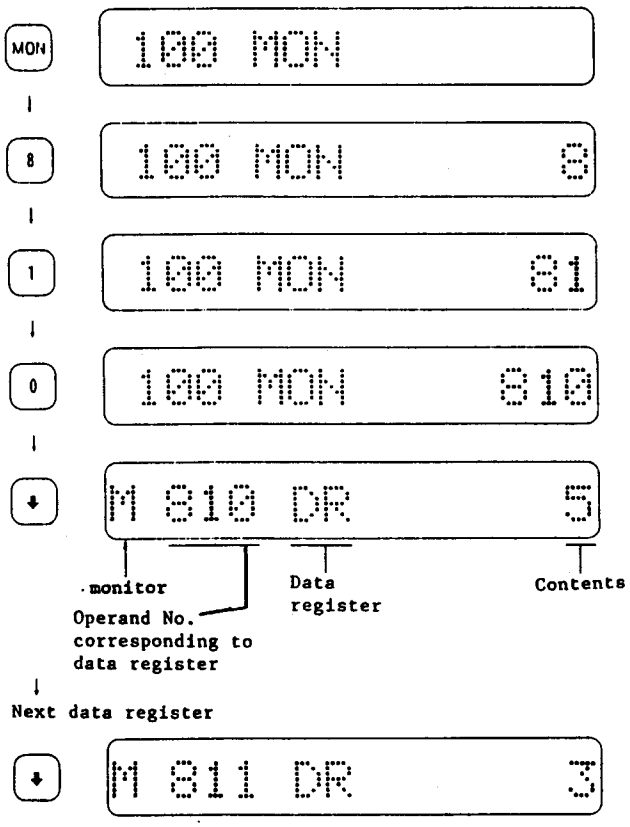
Data registers are read out using operand numbers.

Operation Sequence

MON → Data Register Operand No. → ↓ or ↑

- Key operation and display

[Ex.] To monitor Data Register 10 (DR10).
DR10 monitors Operand No. 810 as shown in the table above.



Supplementary

1. The contents of the data register are displayed in decimal notation.
2. Program loader cannot be used to enter programs into data registers.

Specifications and descriptions in this manual are subject to change without notice.

idec

IDEC IZUMI CORPORATION
7F, Shin-Osaka Mori Bldg., 13-9, Nishinakajima 5-Chome, Yodogawa-ku, Osaka 532, Japan
Phone: (06) 300-5530, Telex: 523-3710, Facsimile: (06) 300-5537

IDEC CORPORATION (USA)
1213 Elko Drive, Sunnyvale, Calif. 94089-2211, U.S.A.
Phone: (408) 747-0550, Telex: 340601
TWX: 910 339 9383, Facsimile: (408) 744-9055

IDEC CANADA LIMITED
Unit 14-7449 Hume Avenue, Delta, British Columbia, V4G 1C3, Canada
Phone: (604) 946-1271, Facsimile: (604) 946-0368

IDEC ELEKTROTECHNIK GMBH
Wendenstraße 331, D-2000 Hamburg 26, W. Germany
Phone: 0 40-25 11 91-93, Telex: 2 164 486, Facsimile: 0 40-25 33 61

IDEC ELECTRONICS LIMITED
Canbury 2000, Unit 12 Elm Crescent, Kingston-Upon-Thames, Surrey KT2 6HJ, UK Phone: 081 549 0737, Facsimile: 081 546 0963

IDEC IZUMI CORPORATION **Hong Kong Office**
Unit 1401, 14F Ashley Centre, 23-25 Ashley Road, Tsimshatsui, Kowloon, Hong Kong
Phone: (852) 721-3823, Telex: 46539, Facsimile: (852) 368-5590

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